On the Impact of MOS transistor's Gate Resistance on CMOS Oscillators beyond 10 GHz operation: Analysis and Design Strategy

Ittipon Kunnapatee
The Electrical Engineering Graduate Program, Faculty of Engineering,
Mahanakorn University of Technology.

Apisak Worapishet
Mahanakorn Microelectronics Research Center (MMRC)
Mahanakorn University of Technology, Nongchok, Bangkok 10530, Thailand
E-mail: apisak@mut.ac.th

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ABSTRACT

The impact of MOS transistors' gate resistance on the phase noise performance of CMOS LC oscillators is investigated. As oscillation frequencies approaches 10 GHz and beyond, the loss due to the gate resistance starts to dominate the total Q factor of the oscillators' LC resonators, degrading the phase noise. A detailed analysis of the Q factor including the gate resistance is given, and this leads to a design strategy to mitigate the impact via the concept of minimum inductance. Simulations of oscillators for the oscillation frequencies ranging from 2 GHz to 32 GHz are provided to verify the impact, and to demonstrate the integrity of the analysis and design strategy.

Keywords: *LC resonator, oscillator, phase noise, Q factor.*

1. INTRODUCTION

The recent advancement of state-of-the-art fine line CMOS processes has brought about a rapid expansion of low cost wireless systems for a wide range of applications. With the quest for more data rates, the operating frequency of wireless systems has been pushed toward higher frequencies, from a few GHz to beyond 30 GHz in the realm of millimeter wave frequencies [1]-[4]. This, as a consequence, requires a voltage-controlled oscillator (VCO) with commensurate performance, specifically the phase noise. The phase noise of VCOs, which critically influences the performance of the entire wireless system, is strongly affected by the quality factor (*Q*-factor) of the LC resonator [5].

At frequencies below 10 GHz, it is well-established that the *Q*-factor of the LC resonator is limited primarily by the losses in the integrated on-chip inductor [5]-[7]. This is no longer the case beyond 10 GHz operation, since recent VCO implementations have clearly indicated a major shift in the component that limits the resonator's *Q*-factor to the MOS varactor [1], [3]. With a proper choice of capacitor ratio and device structure, the impact of the losses in the varactor can be significantly minimized [1]. In fact, another component that starts to play a major role in limiting the *Q* factor is the MOS transistors, but little has been discussed on its adverse impact. It is thus the purpose of this paper to analyze the effect of the loss associated with the MOS transistors, particularly the gate resistance, on the LC resonator's *Q* factor. The loss mechanism in the VCO components is briefly outlined in Section 2. This is followed by the analysis of the *Q* factor which includes the MOS transistor's gate resistance in Section 3. Also outlined in this section is a design strategy based on the concept of minimum inductance to help mitigate such effect, along with discussion on practical considerations. In Section 4, simulation is provided as a verification of the analysis and design. Conclusion is then given in Section 5.

2. VCO 'S COMPONENTS AND LOSS MECHANISM

In general, a VCO is composed of an LC tank resonator and MOS transistors to provide a negative resistance for sustained oscillation condition. Fig. 1 shows the typical circuit schematic of a CMOS VCO using the cross-coupled topology [5]. It can be seen that the LC resonator makes use of the integrated inductor L, the MIM capacitor C_m, and the varactor C_v to enable frequency tenability. The phase noise of the VCO can be optimized by maximizing the total Q factor of the tank resonator. This can be obtained by minimizing the *total* losses associated with each of the tank components. At below 10 GHz, the loss due to the inductor dominates. At beyond 10 GHz however, the losses associated with the capacitive components, particularly from the varactors C_v and the gate capacitance C_g of the MOS transistors start to dominate. In this section, the loss mechanisms and the Q characteristics of these components are briefly discussed where it is aimed to explain how the Q factor of the integrated inductor tend to increase, whereas those of the capacitors C_m, C_v and C_g tend to decrease as we move to higher operating frequencies.

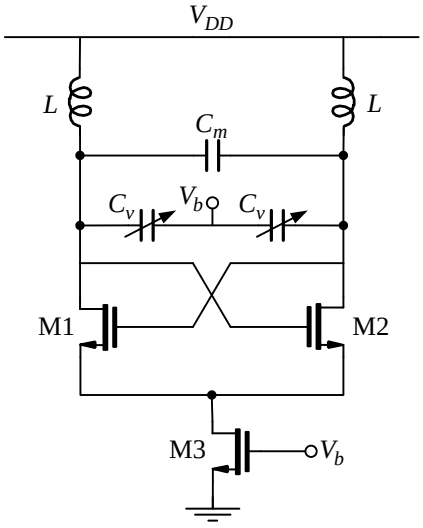


Fig. 1 *Cross-coupled CMOS voltage controlled oscillators.*

2.1 Integrated Inductor

For an inductor, the Q factor is represented by the ratio of the stored magnetic energy over the average loss energy in one period of a sinusoidal signal. For integrated inductors, the parasitic resistances in the metal wire dissipate energy through ohmic loss, while the parasitic capacitances between the metals store unwanted electric energy. In addition, the electric coupling to the semi-conductive silicon substrate causes current to flow, giving rise to substrate loss. At high frequencies, the skin effect and the proximity effect cause a non-uniform current distribution in the metal segments, thereby introducing frequency dependent loss in the metal. The magnetic coupling to the substrate also induces parasitic currents ("eddy currents") in the substrate, adding an additional frequency dependent term in the metal loss.

Fig. 2(a) shows a simple lumped element model of an integrated inductor. The spiral coil itself is modeled by the ideal inductance L_s. The series resistance R_s representing DC and frequency dependent resistive losses in the metal. The inter-wire capacitance C_s is mainly determined by the plate capacitance between the spiral and the underpass. The oxide capacitances C_{ox} and the RC network R_{si} and C_{si} represent the electric field interaction with the substrate.

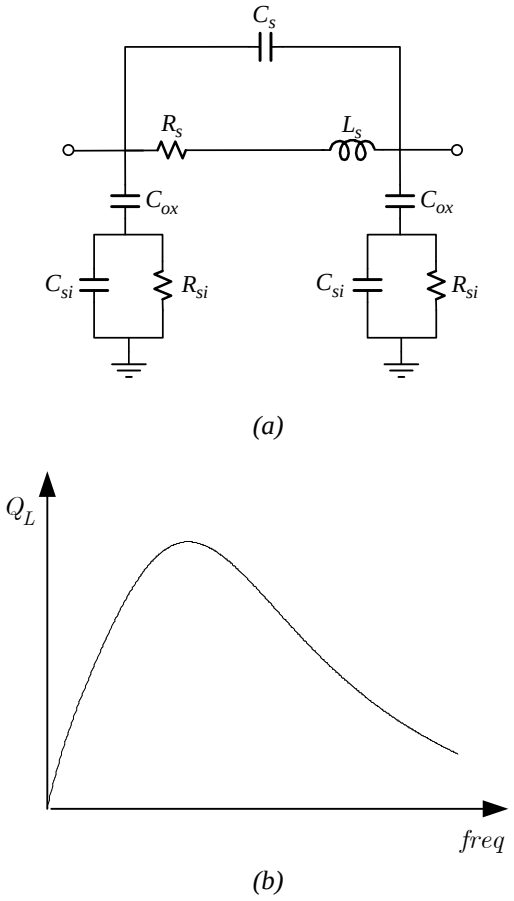


Fig. 2 *(a) Lumped element model of integrated inductor and (b) Q characteristic versus frequency.*

Fig. 2(b) depicts a simulated *Q* characteristic versus frequency of lumped element model of an integrated inductor. At the low frequencies range, the *Q* factor is limited primarily by the ohmic losses in the metal conductor itself, and it increases with frequencies. At the high frequencies range, the *Q* factor starts to decrease with frequencies. This is because more losses appear in the substrate as a consequence of both the electric field which creates conductive current through the substrate, and the magnetic field which induces eddy currents. Thus, for operation at millimeter wave frequencies, inductors must feature a small strip width and a small outer diameter so as to minimize the substrate volume occupied by the electromagnetic field with consequent benefit to minimizing losses. At frequencies near the self-resonant frequency f_{srf}, the *Q* factor decrease dramatically because of the stored magnetic energy is counterbalanced by the unwanted electric energy, and the inductor is turned into a capacitor beyond f_{srf}. The resonant frequency can be also maximized by employing a minimum number of turns to minimize the electric field between the metal turns, and also, maximizing the distance between the metal and the substrate by employing the top metal layer.

2.2 MIM Capacitors

The planar MIM structure is widely used in analog/mixed-signal/RF capacitor, due to an inherent advantage that metal provides depletion-free, high-conductance electrodes suitable for high-speed applications. Its parallel plate structure is formed by a special intermediate metal level just underneath the top metal level of a CMOS process [8]. The MIM capacitor is superior to the poly-poly capacitor structure because the bottom plate is positioned further from the substrate, minimizing parasitic capacitive coupling, and the metal plates are inherently low in resistance.

For a capacitor, its quality factor is represented by the ratio of the stored electric energy over the average loss energy in one signal cycle. In MIM capacitors, the *Q* factor is mainly limited by the ohmic loss from the parasitic resistances at the contacts. Also contributing to the losses is the coupling of the electric field, particularly from the bottom intermediate plate to the substrate.

Fig. 3(a) shows a simple lumped element model of a MIM capacitor. The parallel plate structure is modeled by an ideal capacitance C_s, where a series resistance R_s and a series inductance L_s represent resistive losses and the stored magnetic energy in the metal contacts, respectively. The coupling of the electric field into the substrate is represented by the oxide capacitances C_{ox} and the RC network R_{si}, C_{si}.

Fig. 3(b) depicts the simulated *Q* characteristic versus frequency of lumped element model of the MIM capacitor. The *Q* factor is limited primarily by the ohmic losses in the metal contacts, and it inherently decreases with frequencies. It should be noted that the contacts is made from metal and hence its associated loss is very small, yielding a high *Q* factor. For the self-resonant frequency f_{srf}, it is typically very high since the unwanted stored magnetic field in the MIM capacitor is small.

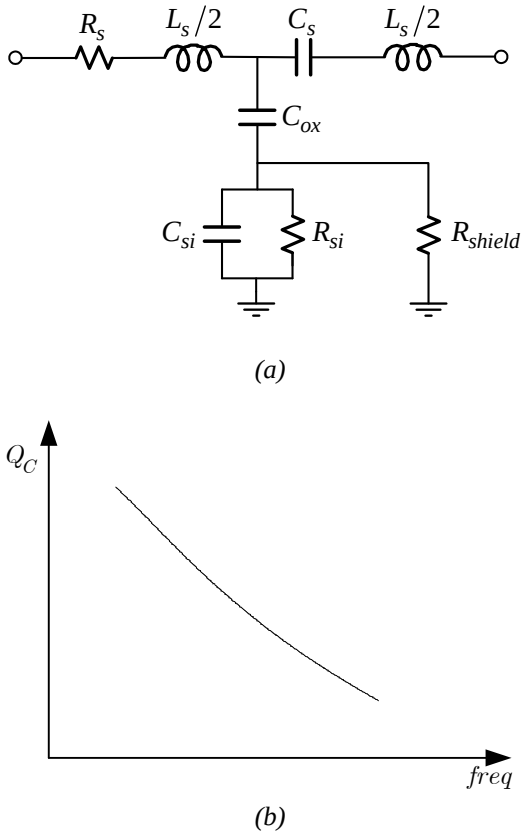


Fig. 3 *(a) Lumped element model of on-chip MIM capacitor and (b) Q characteristic versus frequency.*

2.3 MOS Varactors

Fig. 4 shows the top-view, cross section of a MOS varactor where the top and bottom metal plates are formed by silicided n-polysilicon and n-well, which are separated by a very thin gate-oxide layer for a high capacitance density. The poly gate is connected at two ends to reduce the contact resistance. To increase the tuning range, the parasitic capacitance must be minimized.

The *Q* factor of the MOS varactors is limited by the series resistance of the contacts which has two components: one from the top current path along the silicided poly gate (gate resistance) and the other from the bottom current path along the channel region (channel resistance). Conventional MOS varactors make use of the multi-finger structure for which multiple gate fingers with length and width are connected in parallel to minimize the resistance. External components such as contact resistance and source/drain region series resistance also contribute to the varactor's losses

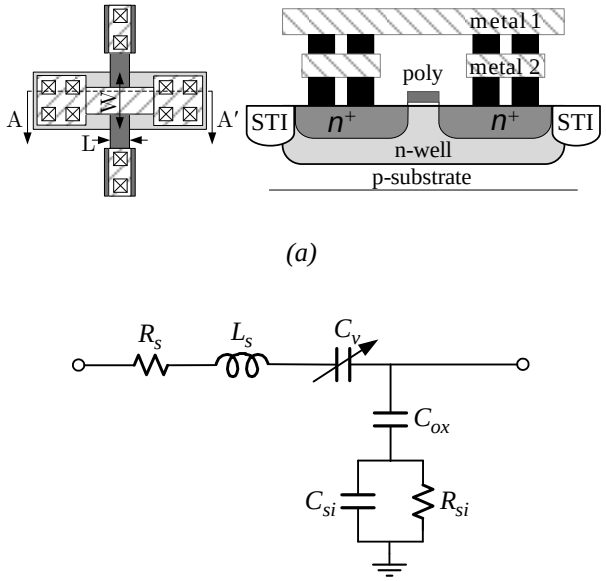


Fig. 4 *(a) Cross section view of MOS varactor, (b) equivalent circuit model.*

A simplified series C_v - R_s - L_s model of the varactor is shown in Fig. 4(b). The gate oxide region mainly contributes to the varactor's capacitance, where the resistance from poly gate and n-well dominate the losses. At high frequencies, the skin effect at the contacts further reduces the *Q* factor.

The *Q* characteristic of the varactor is similar to the MIM capacitor, where it decreases with frequency. However, the contacts resistance is considerably higher and bias dependent, and hence the *Q* value is much smaller than that of the MIM capacitor.

2.4 MOS Transistors

A simplified circuit model of the MOS transistor is shown in Fig. 5. This equivalent circuit is made of the intrinsic part of the devices, including the gate-oxide capacitance C_{ox} and the transconductance g_m. The other elements are parasitic components corresponding to the extrinsic part of the device, including the parasitic capacitances C_{gd}, C_{db}, and the parasitic resistances, R_g and R_{ds}, These parasitcs play an increasingly important role as the operating frequency rises. For the gate resistance R_g in particular, it plays an important role in determining the total *Q* factor of the LC tank in a VCO for mm-wave VCOs. Also, the parasitic capacitance essentially limits the tuning range. Therefore, the parasitic capacitances of the transistor must also be minimized. To minimize the gate resistance, the finger width needs to be kept small. This, however, increases gate-to-body/substrate capacitance. Because of these two competing effects, there should be an optimal finger width.

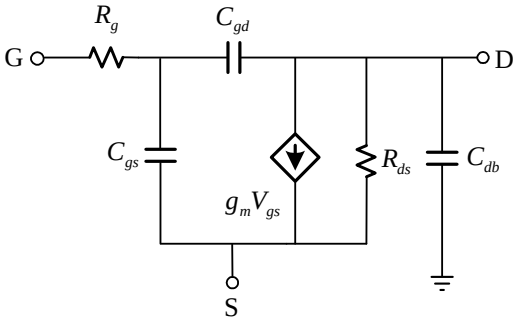


Fig. 5 *Simplified equivalent circuit model of MOS transistors.*

3. *Q*-FACTOR ANALYSIS AND DESIGN STRATEGY

The analysis of the *Q* factor with particular emphasis on the effect of the MOS transistor's gate resistance is given in this section. It is assumed that the *Q* factor of the MIM capacitor is relatively high and can thus be omitted. The loss associated with the MOS varactors is also omitted because it is assumed that the varactor is small and is mainly employed for fine frequency tuning of the VCO, and that the coarse tuning is obtained via switched capacitor bank.

3.1 Analysis of Resonator's *Q* factor

Fig. 6(a) shows the equivalent circuit model of the passive LC tank in the CMOS VCO of Fig. 1, where the series resistors r_{Ls} and r_g represent the total losses in the inductor *L* and the loss due to the gate capacitance C_{gs}, respectively. The capacitor *C* models both the MIM capacitor C_m and varactor C_v. The circuit can be

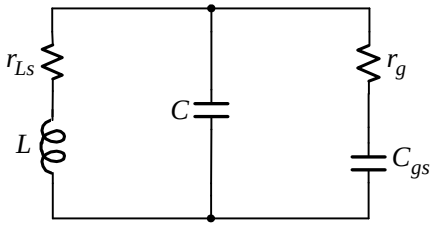
transformed into its equivalent parallel RLC network as shown in Fig. 6 (b), around ω_0, where we have

$$r_{Lp} = r_{Ls}(1+Q_L^2) \tag{1}$$

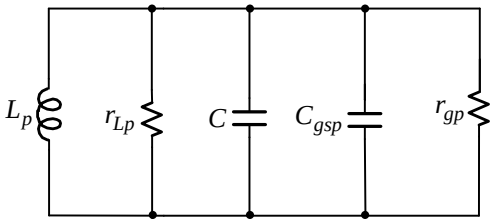
$$L_p = L(1+1/Q_L^2) \tag{2}$$

$$C_{gsp} = C_{gs}/(1+1/Q_C^2) \tag{3}$$

$$r_{gp} = r_g(1+Q_C^2) \tag{4}$$



(a)



(b)

***Fig. 6** (a) Equivalent circuit of LC resonator with gate resistance, (b) transformed circuit model.*

In the equations, $Q_L = \omega_0 L/r_{Ls}$, $Q_C = 1/(\omega_0 r_g C_{gs})$ and $\omega_0 = 1/\sqrt{L_p(C_{gsp}+C)}$. Thus, the total Q factor, Q_T, can be derived as

$$Q_T = \frac{1}{\left(\frac{1}{r_{Lp}}+\frac{1}{r_{gp}}\right)\sqrt{\frac{L_p}{(C_{gsp}+C)}}}$$

$$= \frac{1}{\frac{\omega_0 L_p}{r_{Lp}}+\frac{1}{\omega_0 r_{gp}(C_{gsp}+C)}}$$

$$= \left(\frac{1}{Q'_L}+\frac{1}{Q'_C}\right)^{-1}, \tag{5}$$

where $Q'_L = r_{Lp}/\omega_0 L_p = Q_L$ and $Q'_C = \omega_0 r_{gp}(C_{gsp}+C)$. For Q'_C, it can also be rewritten as

$$Q'_C = \omega_0 r_g C_{gsp}(1+Q_C^2)\left(1+\frac{C}{C_{gsp}}\right)$$

$$= Q_C\ (1+\gamma_C)\ , \tag{6}$$

where $\gamma_C = C/C_{gsp}$. Following this, Q_T can also be expressed by

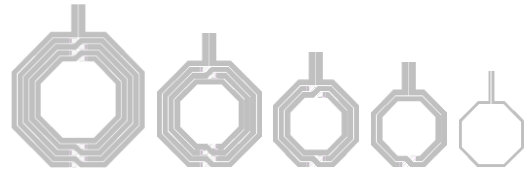
$$Q_T = \left(\frac{1}{Q_L}+\frac{1}{Q_C(1+\gamma_C)}\right)^{-1}. \tag{7}$$

From (7), it can be seen that the total Q factor, Q_T, is dependent on the capacitor ratio $\gamma_C = C/C_{gsp}$. By increasing the ratio, which implies the use of smaller MOS transistors for smaller C_{gsp}, and/or a larger capacitor C, the total Q factor can be increased. It is important to note that a larger C also implies a smaller inductance L_p and hence L for the same oscillation frequency ω_0. Thus, a design strategy deduced from the above analysis is that the inductance L should be minimized in a CMOS VCO so as to mitigate the adverse effect of the gate resistance r_g of the MOS transistors. This has a consequent benefit to increasing the total resonator's Q factor, and hence the phase noise performance.

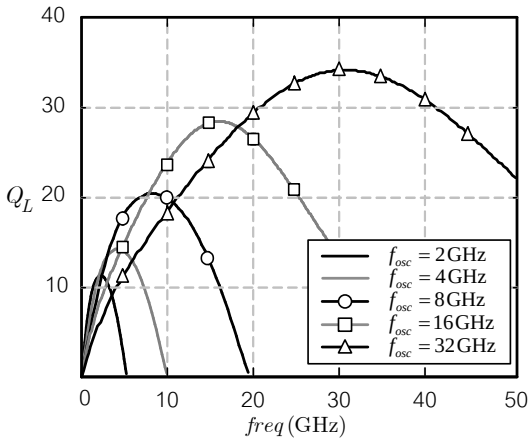
3.2 Practical Discussion

The implication on the use of minimum inductance to mitigate the r_g effect is also in line with the concept of inductance minimization introduced in [5] for VCOs operation where the losses in the integrated inductor dominate. Therefore, the same constraints must be applied. That is the minimum inductance should be selected under the conditions that the oscillation amplitude and startup condition of the VCO are still satisfied for a given bias current.

The use of a minimum inductance also offers a smaller chip area requirement. Moreover, it enables us to extend the current-limited operation of the VCO, and thus the phase noise performance can be further improved by increasing the bias current. This is of particular importance for a very low supply voltage environment in future CMOS processing where the available oscillation amplitude is only in the order of a few hundred milli-volts.



(a)



(b)

***Fig. 7** (a) Inductors' layouts for different oscillation frequencies, (b) simulated Q characteristic.*

***Table 1** Dimension of inductors.*

f_{osc} (GHz)	Width (μm)	Inner diameter (μm)	Turns
2	10	152	5
4	10	118	4
8	10	104	3
16	10	108	2
32	5	120	1

4. SIMULATION RESULTS

In this section, the analysis and the outlined design strategy are demonstrated through designs and simulations of CMOS oscillators operating at 2, 4, 8, 16 and 32 GHz. The employed process is a 6-metal 1.2V 0.13μm CMOS technology. To enable simple comparisons on the impact of the gate resistance on the resonator's Q factor, and the resultant phase noise performance, the dimension and bias current of the MOS transistors were maintained in all the oscillators, with I_{bias} = 2 mA and W/L = 28.8μm/0.13μm. Note that the employed process provides a complete set of RF models and layouts well characterized up to 40 GHz for all the essential circuit components (such as MOS transistors, planar inductors, MOS varactors and MIM capacitors, etc.). To enable full control over the inductors' characteristic, however, the on-chip symmetrical inductors of the oscillators were designed and characterized using a full-wave EM simulator. Agilent-Momentum [9]. All circuit simulations were performed using Agilent ADS [9].

The layouts of the designed inductors and their simulated Q characteristics are depicted in Fig. 7(a) and 7(b), respectively. The inductors dimension are given in Table 1. It is noticed that the peak Q value for each inductor are located near their corresponding oscillation frequency. In addition, a smaller inductor exhibit a higher peak Q factor because the substrate loss and the proximity effect are reduced and the resonant frequency is increased, as described in Section 2.1. Fig. 8 shows the Q factors versus oscillation frequency f_{osc} for the inductors Q_L and the overall capacitors Q'_C which is a combination of the capacitor C and the gate-oxide capacitor C_{gs}. The employed inductance and capacitance versus f_{osc} are given in Table 2, where C_{gs} is fixed at 47.34 fF. As anticipated from Fig. 8, Q_L increases and Q'_C decreases at a higher f_{osc}. More importantly, Q'_C drops below Q_L when f_{osc} approaches 10 GHz and beyond. Also given in the plots are the total Q factors Q_T versus oscillation frequency from both simulation and calculation using (7), where the calculated values agree reasonably well with simulated values. It is evident from the Q_T plots that the total Q factor of the oscillator's resonator drops at 32 GHz operation. This is mainly due to the effect of the gate resistance which significantly reduces the Q'_C value at 32 GHz as also indicated in the figure. By employing the concept of minimum inductance in order to mitigate the effect, the inductance is lower from 0.34 nH to 0.17 nH for the 32 GHz oscillator. This, as a consequence, increases the capacitance C by a factor of ~4, and results in the Q factor of the overall capacitors at Q'_C =29.75. The modified inductor's layout is given in Fig. 9, where it

occupies less chip area by 28%. Also, the Q factor at 32 GHz is simulated at Q_L = 39.45. Thus, by using (7), the simulated total Q factor is now increased from Q_T = 11.25 to Q_T = 18.42. From calculation, the total Q factor is at Q_T =16.96.

Table 2 *Inductance and capacitance vs* f_{osc}.

f_{osc} (GHz)	Inductance (nH)	Capacitance C (fF)
2	8.02	735
4	3.97	343
8	2.01	141
16	1.00	45
32	0.34	24

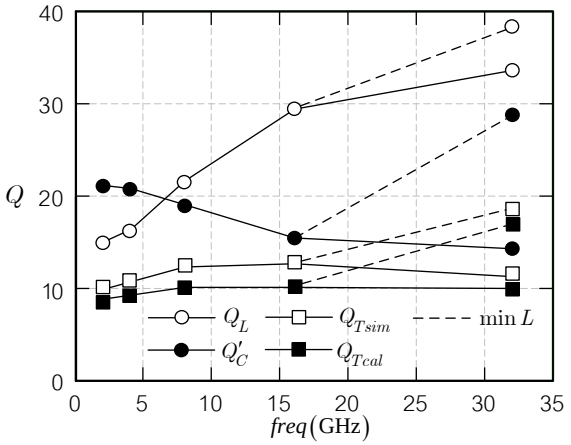


Fig. 8 *Q Factors of inductors, capacitors and resonators at different oscillation frequencies.*

Fig. 9 *Modified inductor layout (dimension width=15µm, inner diameter=80 µm, turns=1) for 32 GHz oscillator.*

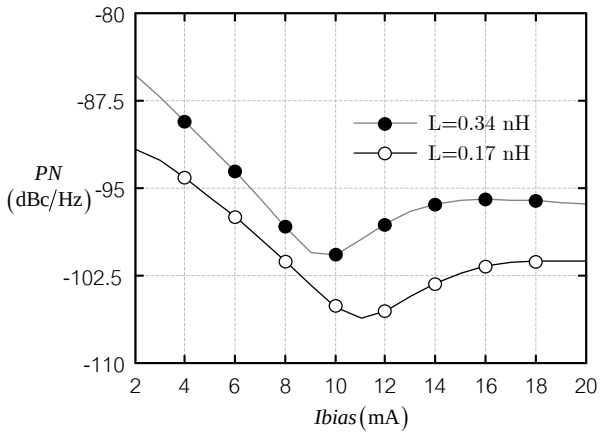


Fig. 10 *Phase noise versus bias current at 1.0 MHz frequency offset for 32 GHz oscillators using 0.34 nH and 0.17 nH inductors.*

Based on phase noise simulation at 32 GHz operation, the oscillator which makes use of the smaller inductance at 0.17 nH exhibits a better phase noise performance by more than 6.36 dB at 10 kHz, and 6.35 dB at 1 MHz offset frequencies at the nominal I_{bias} = **2** mA. This thereby verifies the feasibility of the design strategy in Section 3. Fig. 10 shows the simulated phase noise at 1 MHz offset frequency versus the bias currents for the 32 GHz oscillator with 0.34 nH and 0.17 nH inductors. While the minimum phase noise of the oscillator using 0.34 nH occurs at I_{bias} = 10 mA where the circuit enters voltage-limited regime, the phase noise of the oscillator using 0.17 nH reaches the minimum level at –106.1 dBc/Hz where I_{bias} = 11 mA. This is more than 5.4 dB improvement on the minimum achievable phase noise. Clearly, the use of a smaller inductance not only improves the phase noise, but also extends the operation in the current-limited region and hence the trade-off between the phase noise and the bias current.

5. CONCLUSION

The effects of the MOS transistors' gate resistance on the LC resonator's Q factor and the phase noise of CMOS oscillators have been studied. The frequency characteristics of the Q factors have been discussed for each building components of the oscillators. An analysis of the Q factors including the loss from the gate resistance which becomes dominant at frequencies beyond 10 GHz has been derived. A design strategy based on the concept minimum inductance and higher Q factor have been introduced to suppress the loss. Based on simulation of the 32 GHz oscillator, the concept

yielded improvement in the total *Q* factor by a factor of 1.6 and the phase noise by more than 6.35 dB, as well as the minimum achievable phase noise by 5.4 dB, at larger bias current by only 10%.

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Ittipon Kunnapatee received the B.Eng. degree in Telecommunication Engineering from Suranaree University of Technology, in 2007. He is currently working toward the M.Eng. degree in Electrical Engineering at Mahanakorn University of Technology.

Apisak Worapishet received the B.Eng. degree (with first-class honors) from King Mongkut's Institute of Technology Ladkrabang, Bangkok, Thailand, in 1990, the M.Eng.Sc. degree from the University of New South Wales, Australia, in 1995, and the Ph.D. degree from Imperial College, London, U.K., in 2000, all in electrical engineering. Since 1990, he has been with Mahanakorn University of Technology, Bangkok, Thailand, where he currently serves as the Director of Mahanakorn Microelectronics Research Center (MMRC) and he Associate Professor with Telecommunication Department. His current research interest includes mixed-signal CMOS analog integrated circuits, wirelined and wireless RF CMOS circuits, microwave circuits, and reconfigurable communication systems.