A Very Low Voltage Mixer for Baseband Wireless Sensor Applications

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ABSTRACT

An enhanced mixer topology suitable for very low supply voltage applications is developed. The circuit introduces a linear resistor network to the conventional mixer based on cross-coupled triode MOS transistors to render extended transistors' operation and linearity improvement at a low supply. Detailed analysis that leads to a systematic design is outlined. The feasibility of the mixer for baseband wireless sensor applications is demonstrated through simulation of a 0.5-V demodulator for IEEE 802.15.4 radio using regular transistors in a 1.8V 0.18µm CMOS process with V_{T0} = 0.4V which is as large as 80% of the supply voltage. Also provided to verify its practicality is the experimental demodulator at a reduced data rate based upon a breadboard implementation using array transistors.

Keywords: *Low voltage circuits, sub-threshold circuits, FSK demodulator*

1. INTRODUCTION

With potential applications in environmental monitoring, surveillance, health-care, security etc, wireless sensor networks have been envisaged as holding promise for future ubiquitous wireless computing systems. Among the essentials to a full scale deployment of such sensor networks are analogue techniques that can enable efficient operation at a very restricted supply voltage level. In response to this demand, various innovative circuits fully compatible with an ultra-low supply voltage in nanoscale CMOS have been demonstrated. These include an OTA for filter applications [1], [2], passive analogue sampling circuits [3], [4], and an active track-and-hold circuit [5] for ADC applications − all operating at a 0.5-V supply voltage using standard transistors. Also developed were techniques for time-constant tuning based upon variable capacitors [2] and sub-threshold MOSFET operation [1], [6], [7]. To complement the ultra-low supply scenario, a circuit arrangement for a mixer with a commensurate supply voltage requirement is introduced in this letter, with the targeted application for baseband demodulators of wireless sensor transceivers.

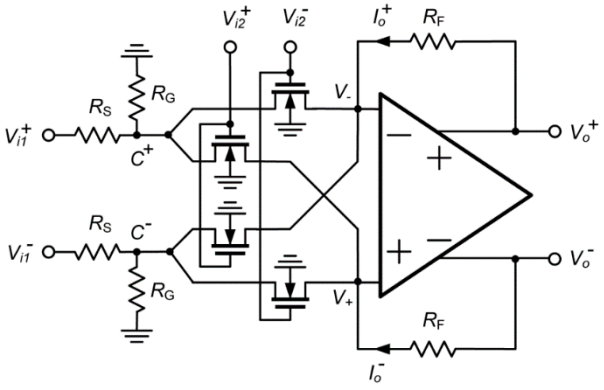

Fig. 1 Very low voltage mixer topology.

2. CIRCUIT STRUCTURE

Traditionally, a mixer topology for down-conversion and baseband applications makes use of four cross-coupled MOS transistors operated in strong inversion and triode region, with one of their drain/source terminals connected to a virtual ground [8], [9]. At a reduced supply voltage however, such a topology shares a similar difficulty to conventional tunable MOS resistors for integrated continuous-time filters [2]. Both require excessive headroom, particularly for the input

voltages at the gate terminals, so as to keep the transistors in their strong triode operation at all times. Thus, without the use of a charge pump which may entail a reliability issue, the quad MOS transistors can be pushed into subthreshold conduction, especially at the negative swing of the gate inputs. In effect, the mixer is turned to operate in a current commutation manner, where each of the transistor pairs takes turn to conduct during each half of the input cycle. This in turn degrades the linearity since the dependence of g_{DS} on V_{DS} is now highly nonlinear and can no longer be suppressed by virtue of the double-balanced structure [7]. Moreover, the conversion gain of the mixer is degraded due to a significant reduction of g_{DS} at sub-threshold conduction. With a continued supply reduction to a very low voltage, the mixer may cease to operate entirely. Fig. 1 shows an enhanced low-voltage mixer topology where it resembles the conventional triode-biased mixer in [8], [9], but with the incorporation of the linear resistors RS and RG at the drain/source terminals of the quad transistors. In the circuit, one of the differential input signals is applied at the resistors' terminals, $V_{i1}^{+/-}$, and the other at the transistors' gates, $V_{i2}^{+/-}$. The mixing output current $I_o^{+/-}$ is converted to the differential voltage, $V_o^{+/-}$, by the feedback resistors RF . The resistor network serves as a voltage division that essentially pulls down the drain/source terminals of the quad MOS transistors below the quiescent bias voltage of $V_{i1}^{+/-}$ (typically at a mid-supply level), thereby enlarging the gate overdrives and pushing the devices' operation back towards strong inversion. In addition, R_S and R_G together form an equivalent linear resistor in series with the quad transistors, yielding a significant improvement in the linearity as it helps suppress the effect of the nonlinear g_{DS}–V_{DS} characteristics contributed by the transistors, especially when they are in sub-threshold conduction. It is worth noting that the grounded resistors R_G in Fig. 1 can be replaced by a current source to produce a similar extended operation in the transistors, but this is not the choice here due to the associated flicker noise.

3. MIXER DESIGN

Of prime importance is a careful design methodology of the very low voltage mixer, due to a limited available signal swing at a low supply voltage. Also, due to such a wide coverage of the MOSFET's operation, it is obliged to employ a general current-voltage MOS equation valid for all regions in the analysis. This may be given by [10]:

$$I_{DS} = 2m\varphi_t^2\beta\left\{\ln^2\left(1+e^{\frac{V_{GB}-V_{T0}-mV_{SB}}{2m\varphi_t}}\right)-\ln^2\left(1+e^{\frac{V_{GB}-V_{T0}-mV_{DB}}{2m\varphi_t}}\right)\right\}$$

with

$$m=\left(1-\gamma\,/\,2\sqrt{V_{GB}-V_{T0}+\left(\gamma\,/\,2+\sqrt{\varphi_0}\right)^2}\right)^{-1} \quad (1)$$

where $\beta = \mu C_{ox}$W/L is the transconductance parameter, $\varphi_t = kT/q$ is the thermal voltage, μ is the carrier effective mobility in the channel, C_{ox} is the gate-oxide per unit area, W and L are the channel width and length, V_{T0} is the threshold voltage at $V_{SB} = 0$, γ is the body effect coefficient, φ_0 is a characteristic potential, and m is the slope factor. It is noted that the shortchannel effects and the dependence of the mobility on the transversal field are not included in (1). By using (1), and applying KCL at the common node C^+ or C^- ($C^{+/-}$) of the circuit in Fig. 1, the following normalized equation can be obtained:

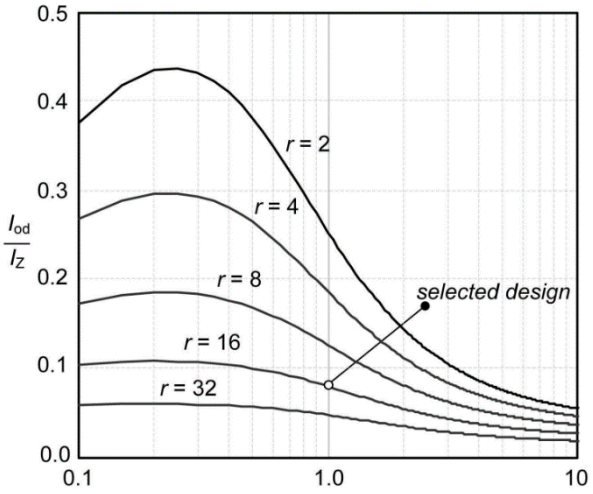

Fig. 2 *Plot of the normalized differential peak output current versus the design parameters r and α.*

$$\frac{v_{i1}^{+/-}-v_C^{+/-}}{r}=\frac{v_C^{+/-}}{\alpha r}$$
$$-\left[\ln^2\left(1+e^{v_{i2}^{+}-v_T-mv_C^{+/-}}\right)-\ln^2\left(1+e^{v_{i2}^{+}-v_T-mv_{+/-}}\right)\right]$$
$$-\left[\ln^2\left(1+e^{v_{i2}^{-}-v_T-mv_C^{+/-}}\right)-\ln^2\left(1+e^{v_{i2}^{-}-v_T-mv_{-/+}}\right)\right] \quad (2)$$

where the input voltages $V_{i1,2}^{+/-}$, the common node's voltages $V_C^{+/-}$, the threshold voltage V_{T0}, and the opamp's input voltages $V^{+/-}$ [cf. Fig. 1] are all divided

by $2m\varphi_t$ to form the normalized variables $v_{i1,2}^{+/-}$, $v_C^{+/-}$, v_T, and $v^{+/-}$ in (2), respectively. Also, $\alpha = R_G/R_S$ and $r = R_S\beta\varphi_t$. Note that the normalization yields the closed-form equation in (2) which facilitates a systematic design as will be shortly described. Given a set of dc bias and input signal levels, one can determine $V_C^{+/-}$ based on numerical computation of (2). Subsequently, the normalized mixer's output currents $I_o^{+/-}/I_Z$, where $I_Z = 2m\varphi_t^2\beta$, can be calculated as

$$\frac{I_o^{+/-}}{I_Z} = -\left[\ln^2\left(1+e^{v_{i2}^{+}-v_T-mv_C^{-/+}}\right)-\ln^2\left(1+e^{v_{i2}^{+}-v_T-mv_{-/+}}\right)\right] + \left[\ln^2\left(1+e^{v_{i2}^{-}-v_T-mv_C^{+/-}}\right)-\ln^2\left(1+e^{v_{i2}^{-}-v_T-mv_{-/+}}\right)\right] \quad (3)$$

For a particular set of conditions compatible with values assigned in the subsequent simulation, the numerical plot of the normalized differential peak output current, $\hat{I}_{od}^{+/-}/I_Z = (\hat{I}_o^{+} - \hat{I}_o^{-})/I_Z$ can be determined using (3). This is given in Fig. 2 as a function of the design parameters $\alpha = R_G/R_S$ and $r = R_S\beta\varphi_t$. The plot indicates that, for a large α and a constant r, the output peak current increases with a successive reduction of α. This trend holds until around α = 0.2 to 0.3 where only a marginal improvement or even a drop in the output is obtained. For a constant α, a smaller r results in a larger output but this cannot be reduced in-definitely since a smaller r results in smaller R_S and hence R_G, and there exists a limit determined by the driving capability of the preceding stage. These considerations will be employed for the mixer design in the next section.

4. DESIGN AND PERFORMANCE VERIFICATION

The mixer in Fig. 1 has been designed and simulated using a 1.8V 0.18µm CMOS process. The supply voltage was set at 0.5V and the dc bias voltages for $V_{i1,2}^{+/-}$ were both at 0.25V. The differential peak inputs were at $\hat{V}_{id1} = \hat{V}_{i1}^{+} - \hat{V}_{i1}^{-}$ = 0.2V$_p$, and $\hat{V}_{id2} = \hat{V}_{i2}^{+} - \hat{V}_{i2}^{-}$ = 0.4V$_p$. The opamp configuration similar to [2] was employed where the dc bias of its input terminals was set at $V^+ = V^- = 0.4$V. In order to demonstrate a very low voltage capability, the standard n-channel devices were used with W/L= 110µm/1.1µm. As extracted from simulation, this yields β = 25mA/V^2 (I_Z = 45.6μA and $1/\beta\varphi_t = 1.55$kΩ) and $V_{T0} \approx 0.4$V. Based on Fig. 2, for the design case at r = 16 and α = 1.0, $R_S = R_G = 16/\beta\varphi_t \approx$ 25kΩ were determined. This also results in the normalized differential peak output current at $I_{od}/I_Z =$ 0.08. With R_F = 55kΩ, the differential peak output voltage, $\hat{V}_{od} = \hat{V}_o^{+} - \hat{V}_o^{-}$, is at $|\hat{V}_{od}| = |\hat{I}_{od}R_F| \approx$ 0.2Vp. Since we have $\hat{V}_{id1}$ = 0.2V$_p$, the conversion gain is $G = |\hat{V}_{od}/\hat{V}_{id1}| =$ 1.0V/V. Fig. 3(a) shows the simulated waveform (solid line) at the mixer's differential output for a 2MHz high frequency input at $V_{i1}^{+/-}$ and a 50kHz low frequency input at $V_{i2}^{+/-}$. The resulting output differential peak voltage is at 0.2V$_p$, yielding the down conversion gain at G = 1.0V/V. Also given in the plot is the mixer's output with R_G in Fig. 1 removed (gray line), i.e., α approaches infinity, where it is seen that the amplitude and hence the gain drops significantly by more than five folds. It should be noted that simulations of the mixer with other sets of the parameters, i.e. r ranging from 2 to 32, and α from 0.5 to 2.0 [cf. Fig. 2], were also conducted and the resulting conversion gain exhibit good agreement with the theoretical analysis throughout.

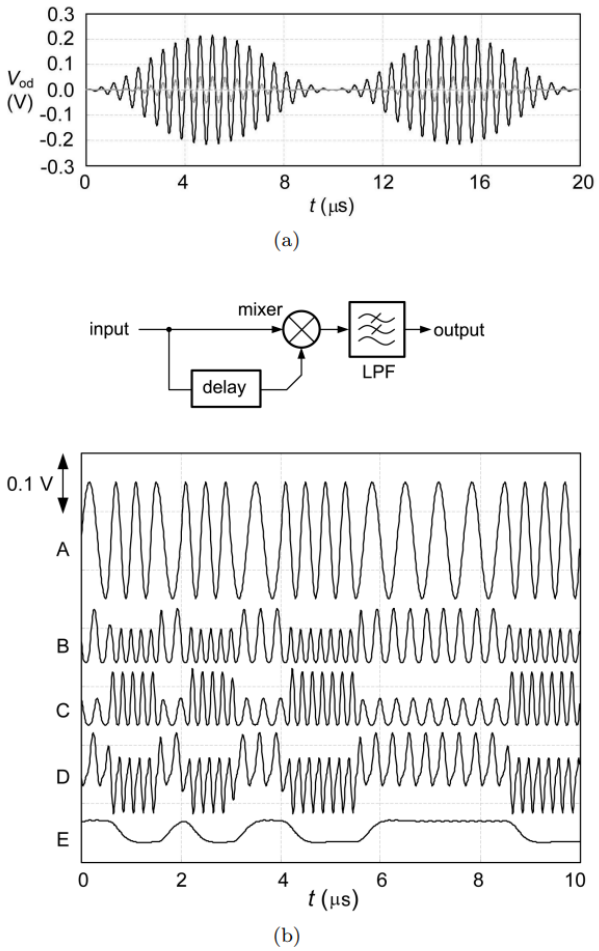

Fig. 3 *Simulated waveforms of (a) mixer with 50kHz and 2.0MHz inputs and (b) 2-FSK demodulator in [11].*

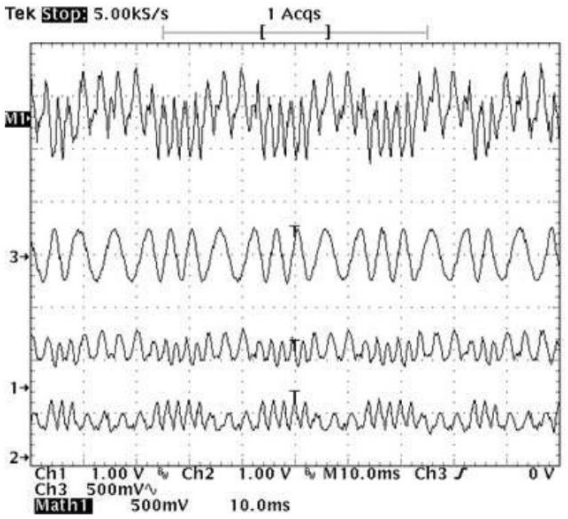

Fig. 4 *Measured waveforms for experimental 2-FSK demodulator using transistor arrays.*

The effectiveness of the designed mixer for use in a baseband application at a 0.5-V supply was also validated. It was employed as a mixer block in the differential delay demodulator for a low-IF IEEE 802.15.4 receiver which is shown in [11] to exhibit superior performance as compared to conventional derivative counterpart. The schematic of differential delay demodulator is as depicted in Fig. 3(b)) with the delay at $-\pi/2$ phase shift for the low-IF of 2.0MHz. A 2-FSK modulated signal (a combination of I- and Q- O-QPSK signals compliant with IEEE 802.15.4 standard) was applied. Fig. 3 shows the simulated waveforms of the demodulator for the 1.5/2.5MHz FSK input at 2Mchip/s (trace A), the single-ended and differential outputs of the mixer (traces B, C and D), and the filtered output (trace E). The filtered output matches well to that obtained from the ideal demodulator where the mixer was replaced by an ideal multiplier with the same conversion gain. The mixer topology was also tested via a breadboard implementation using the n-channel transistor array ALD1106 with $V_{T0} \approx 0.65$V. The opamp was realized by off-the-shelf components. The dc bias voltages of the input terminals were set at $V_{i1}^{+/-} = 0.5$V and $V_{i2}^{+/-} = 0.7$V which is only 50mV above V_{T0}. The peak signal voltage for both inputs is at $V_{i1,i2}^{+/-} = 0.5\text{V}_\text{p}$. The mixer was employed in a reduced-rate demodulator similar to Fig. 3(b) but without the LPF, and the measured waveforms are given in Fig. 4. Trace A is the FSK input, traces B and C are the measured single-ended outputs, and trace D is the differential output after the mixer. It is noticed that the waveforms of Fig. 4 match well to their corresponding waveforms in Fig. 3(b), and thus the functionality of the demodulator implemented by the mixer is verified in practice.

5. CONCLUSION

A very low voltage opamp-based mixer incorporating a linear resistor network to extend the operation of the cross-coupled triode transistors has been presented. Detailed analysis, design and verification have been provided. Its viability has been demonstrated via simulation and experiment where it has made possible an FSK demodulator's operation at a very restricted supply of 0.5V using standard transistors in a 1.8V 0.18μm CMOS. It should be noted that the technique is also readily applicable to extend the operation of the subthreshold MOS resistor technique in [6], [7].

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