Back-to-Back Matching Network Implementation Technique for Accurate Characterization of Source/Load Impedance Seen by Power Transistor in RF Power Amplifier Design

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ABSTRACT

This paper presents a simple and more accurate measurement of matching network characteristics for an RF power amplifier, specifically its driving point impedances as seen by the power transistor, which are critical to its operational performances. The proposed technique relies on an implementation using the same matching network connected in a back-to-back configuration to avoid direct measurement on the matching network port that is connected to the power transistor, which has a relatively large pad size so as to connect with the gate and drain terminals of the power transistor package. This serves to mitigate an interconnect discontinuity between the matching layout and the 50-ohm transmission line layout to a network analyzer. The measured responses based on the back-to-back implementation is then employed to optimize the component values of the matching network schematic so as to fit the measurement with simulation, thereby enabling the implementation of the schematic to more accurately determine the driving point impedance. Validation of the technique is given via practical design and implementation of a 3.1-GHz GAN power amplifier.

Keywords: *RF power amplifier, matching network, measurement technique*

1. INTRODUCTION

Radio frequency (RF) power amplifier is a crucial building element for determining reliable communication distance in a wireless system [1], [2]. Practical design of class AB power amplifier is well established [3], [4]. It involves the use of a nonlinear power transistor model, obtained from either the manufacturer's data sheet or real measurement, to calculate its large-signal and harmonic characteristics and optimal quiescent point for balances efficiency and linearity under the desired class of operation. The subsequently S-parameters are employed to evaluate the amplifier's stability, as well as the load and source pull characteristics for optimum power gain, output power and power added efficiency (PAE) across the operating frequency range. Next, the optimum load and source impedances for the desired gain and performance are determined and their associate matching networks with additional components for gate/drain DC biasing and suppression of harmonic contents are designed. Large-signal simulations of the power amplifier are then performed, and the component values in the input/output matching networks, as well as the bias network are adjusted, if necessary.

Having completed the schematic design, the physical layout is created, which includes transmission lines and pads for lump components, and electromagnetic (EM) simulation on the layout is conducted to account for parasitic effects not included in the initial circuit simulation. Based on the EM simulation result, the layout geometries and component values are adjusted to meet all performance specifications including power, efficiency, and linearity characteristics. The power amplifier board is then implemented and its performance is subsequently measured. Ultimately, the component values or layout geometries of the board may need fine

adjustment to obtain a closer match between the measurement and simulation.

Although the aforementioned practical design procedure is well recognized, there is one hidden issue faced by the designers, which, more than often, leads to off-target performances between simulation and measurement. In particular, due to the parasitic in passive components and tolerances in practical PCB implementation at RF frequencies, there is no warrant that the source and load impedances, as seen by the power transistors will be close to the desired final values, i.e., after the EM simulation. An obvious solution to check such a discrepancy is to actually perform measurement of the input and output matching before assembling the amplifier. However, the main bottleneck here with real PCB measurement of a matching network on the transistor sides stems from a typically large trace width of the PCB footprint for soldering power transistor gate and drain terminals. In particular, this can cause severe discontinuity, both in terms of physical dimension and field pattern, as well as characteristic impedance, if a 50-ohm interconnect transmission line typically employed by a network analyzer is directly connected to such a wide trace. Consequently, the obtained measurement results of the implemented matching network may be highly inaccurate and deviate significantly from the actual source and load impedances, Z_S and Z_L as seen by the power transistors. In order to circumvent this issue, this work proposes a technique based upon a two-port measurement of the back-to-back implementation of two identical matching networks under test, either input or output. The measured two-port parameter is then employed for component optimization of the associated matching network model so that the driving-point impedance seen from half of the back-to-back circuit can be deduced. This leads to no impact from the discontinuities on the wide trace footprint on the transistor side. The technique will be described in detail in the following sections.

2. BACK-TO-BACK MATCHING IMPLEMENTATION FOR IMPEDANCE CHARACTERIZATION

The actual measurement of Z_S and Z_L of the implemented matching circuit is vital to ensure that the performance of the designed PA is in line with simulation. The benefit from actual measurement is to allow us to identify the real cause of discrepancy, if present. This can be from PCB manufacturing tolerances, non-ideal parasitic capacitance, via inductance etc. Once identified, it can be corrected for improved PA performances.

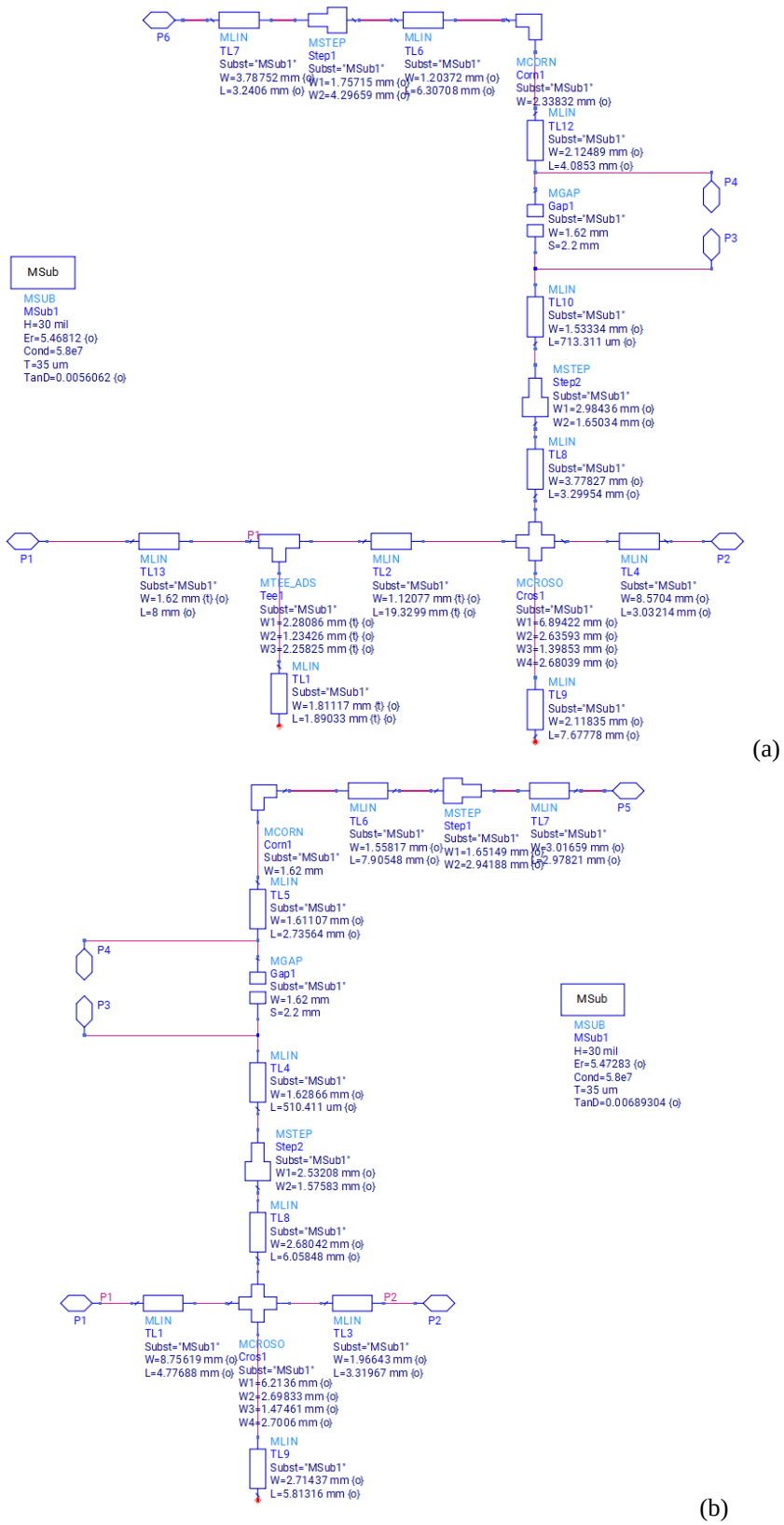


Fig. 1 *Optimized circuit schematic for (a) input matching network and (b) output matching network.*

The proposed technique makes use of the back-to-back implementation of two identical matching networks under test. Specially, its measured two-port S-parameters is employed, to optimize the parameter values of the associated transmission-line and lump-component matching network along with the SMA model in circuit simulation to fit the responses with the measurement.

One clear advantage from the implementation of a back-to-back network is that there are no size and impedance discontinuities from the 50-ohm line access to the network analyzer on both sizes, maintaining accurate measurement results. Typical parameters in the matching circuit for optimization includes the width and length of associated transmission line and open/short stubs, which can be varied due to PCB manufacturing tolerances. Also, this adjustment can serve to partially address the inaccuracy of the lump component model, specifically the component pads and junctions, as compared to full EM simulation. The PCB parameters, such as trace width, length and dielectric properties are also included to account for manufacturing tolerances, with constraints over the range of their relevant practical values.

Other factors that can cause discrepancy between measured and simulated results in the matching circuit include parasitic from capacitor, resistor, inductor, as well as attenuation and phase shift from the SMAs, are also included for optimization with limited range set by their tolerances.

Note that only fitting of responses between measurement and simulation is the main criterion, not the resulting parameters after optimization. The one side of the fitted matching network can now represent real measured results for the actual source and load impedances seen by the power transistors. Without concerning their absolute values, its associated component model parameters in the optimized schematic can also be incrementally adjusted to investigate possible fine adjustment of some component dimensions to achieve a better match between the designed Z_S and Z_L, and the actual values obtained from real PCB implementation, if the current results are still not satisfactory.

3. IMPLEMENTATION AND VALIDATION

3.1 DESIGN AND IMPLEMENTATION

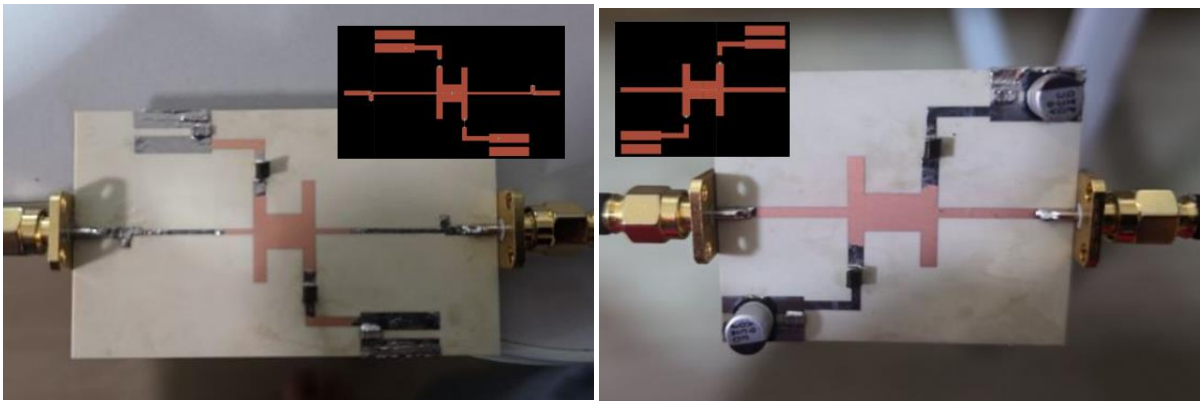
A single-ended Class-AB GaN power amplifier was designed to deliver +12 dB power gain and +42 dBm output power at a 3.1-GHz center frequency and >100 MHz bandwidth. The active device is a MACOM GaN HEMT (CG2H40045) [5], biased at 28-V drain and –3.1-V gate voltages for a class AB operation to balance efficiency and linearity.

The circuit was fabricated on Rogers RO4350 (ε_r = 3.48, tan δ = 0.0037, thickness = 0.762 mm). Both input and output matching networks were realized using microstrip lines and optimized from for |S21| >+12dB power gain and |S11|, |S22| < −10 dB, with unconditional stability over the operating bandwidth [6], [7]. The schematic of the optimized matching networks can be shown in Fig. 1(a) and 1(b).

3.2 MEASUREMENT OF SOURCE AND LOAD IMPEDANCES

Based on the schematic of Fig. 1, the input and output matching networks were subsequently laid out and implemented in a back-to-back fashion as shown in Fig. 2(a) and 2(b). The S-parameters of the back-to-back circuits were measured by using a network analyzer over 2 to 4 GHz, as shown by the black solid lines on Smith chart in Fig. 3(a) and 3(b) for the input and output matching, respectively. As previously outlined, the measured two-port S-parameters were then employed to adjust the component values of the associated transmission-line matching network along with the SMA model in circuit simulation to fit the measured and simulated responses over the frequency range. Also shown in Fig. 3 by the blue solid lines are the simulated S-parameters after the parameter fitting.

Having obtained the fitted component values, the back-to-back input and output matching schematics were then separated back into their corresponding one side. Following this, their input S-parameters with a 50-ohm termination on the opposite side can be simulated as indicated by the red solid lines in Fig. 4(a) and 4(b), and hence the source and load impedance seen by the power transistors are now determined. Also included for comparison are the input S-parameters from full EM simulation of the input and output matching layouts as indicated by the black solid lines in the figure. Agreement between extracted source/load impedances from measurement using the back-to-back technique and EM simulation is clearly observed. This suggests that the characteristic of the implemented input/output matching networks are validated, and they are ready for the PA implementation.



(a) (b)

Fig. 2 *Back-to-back PCB implementation for (a) (a) input matching network and (b) output matching network. Also shown (insets) are their corresponding layouts.*

3.3 MEASUREMENT RESULTS

The realized power amplifier circuit is shown in Fig. 5(a), and the measured S-parameters are given in Fig. 5(b) for S21, S12, and Fig. 5(c) for S11, S22. The amplifier achieved >+12 dB gain at 3.1 GHz with input/output return losses below −10 dB over a 100-MHz bandwidth as required by the design specification. Large-signal measurement shows that the output power reached the 1-dB compression point at +43.1dBm.

4. CONCLUSION

This work has presented the implementation of the back-to-back input/output matching network for more accurate measurement and subsequent extraction of source/load impedance seen by RF power transistor via circuit component optimization. It has been clearly demonstrated that the technique has enabled measurement validation of the input and output networks for a 3.1-GHz GAN power amplifier, where the designed source and load impedances were shown to be in close agreement with the characteristics obtained from EM simulation obtained during the design phase. Following this, the power amplifier was implemented and its performance was measured and verified to be in good agreement with design specification and simulation.

5. ACKNOWLEDGEMENT

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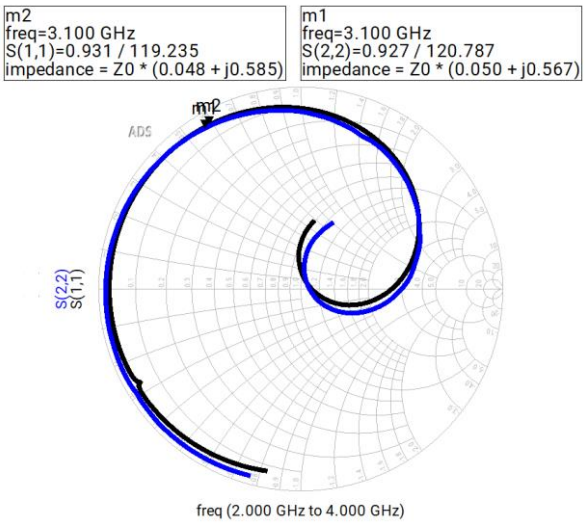
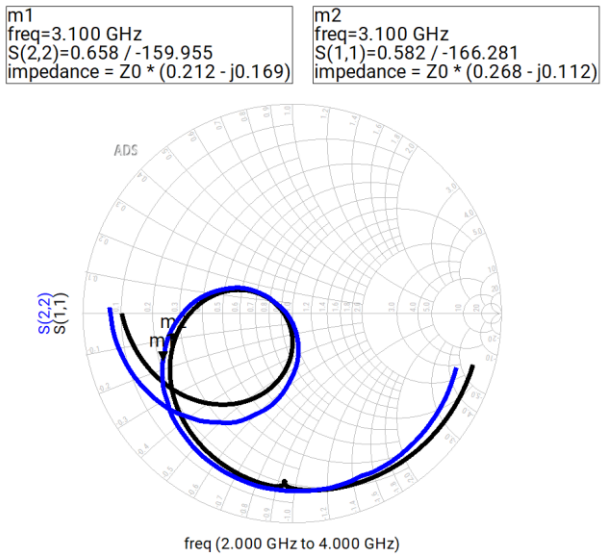
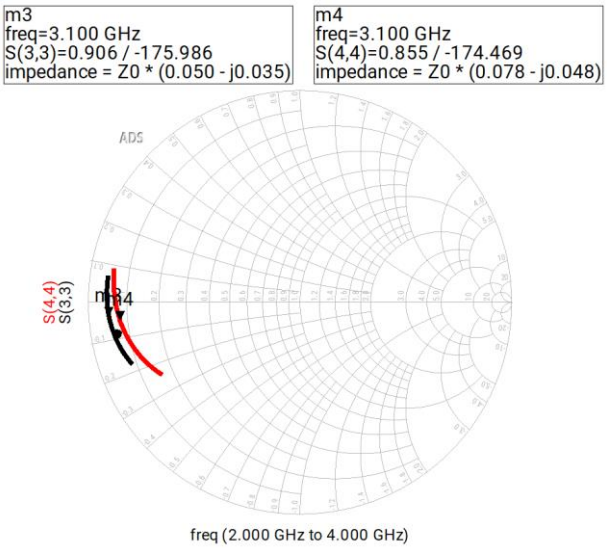


(a)



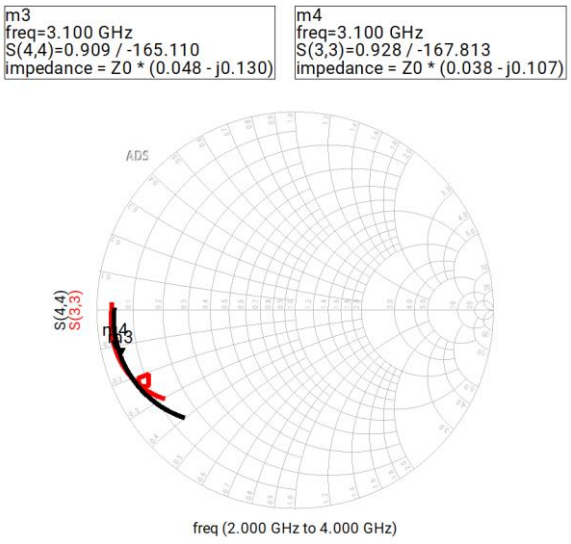
(b)

Fig. 3 *S-parameters after fitting between measurement (black) and simulation (blue) for (a) back-to-back input matching and (b) back-to-back output matching networks.*

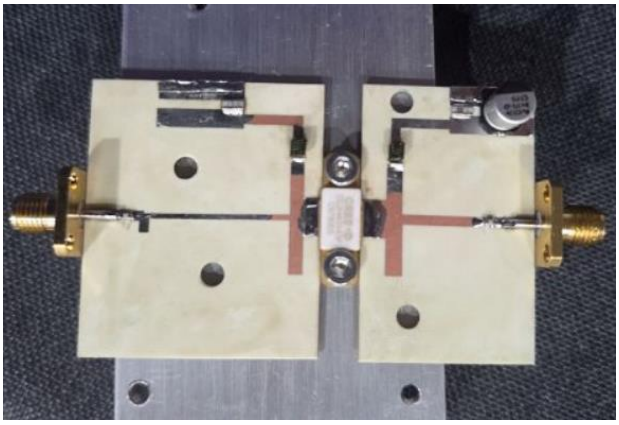


(b)

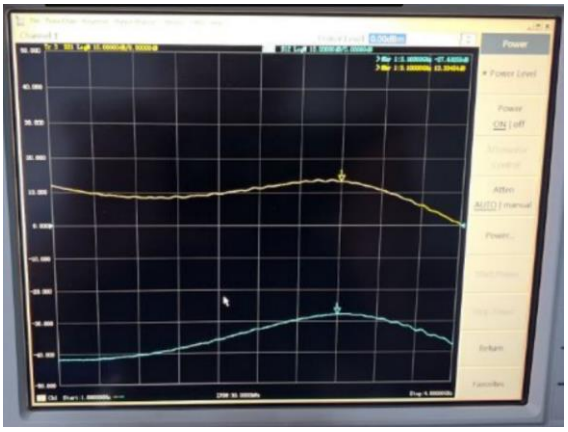
Fig. 4 *S-parameters of (a) input matching and (b) output matching networks with 50-ohm termination as seen by power transistor after fitting between EM simulation (black) and extracted measurement (red).*



(a)



(a)



(b)

(c)

Fig. 5 *(a) Practical PA implementation (b) display of S21 and S12 in dB, and (c) display of S11 and S22 on Smith chart.*

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