E-ISSN 2586-9027
Homepage : https://tci-thaijo.org/index.php/SciTechAsia Science & Technology Asia
Vol.30 No.1 January - March 2025 Page: [189-200]
Original research article

Investigation and Design of T-Type Inverter for Power Distribution Network

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Received 25 April 2024; Received in revised form 1 March 2025
Accepted 17 March 2025; Available online 24 March 2025

ABSTRACT

Green energy and clean power are the recent trends of modern power distribution networks (PDN). In recent years, great attention has been focused on T type inverters due to their advantages over conventional voltage source inverters (VSI), such as fault-tolerant, overload capability, less total harmonic distortion (THD), better output waveform and high efficiency. An inductor coupled T type (IC-T type) inverter-based distribution static compensator (DSTATCOM) is built for active power filtering of 3-phase 3-wire PDN connected nonlinear load in this paper. The proposed topology is composed of three inductors connected between the VSI and common source. The proposed PDN is obstructed by the DSTATCOM using icos□ control algorithm for the inverter DC link voltage reduction, filter inductor rating minimization, decreasing the switching stress, increasing the life span of an inverter, reliable operation, stress balancing, loss reduction and increase in efficiency. Apart from these, other improvements such as power factor (PF) correction, better voltage regulation, harmonics reduction and load balancing are obtained. The efficacy of the IC-T type inverter in different loading scenarios is justified using MATLAB/Simulink software captivating in reflection of the IEEE-514-2017 and IEC- 61000-1-3 benchmark.

Keywords: DSTATCOM; IC-T type inverter; $i\cos\phi$ control algorithm; THD

1. Introduction

With the rapid increase of both industrial and domestic clients, the demand for quality and continuous electricity distribution has gradually increased [1-3]. The quality of power dropped due to the utilization of various nonlinear loads and the application of semiconductor technology in every sector of life by different power consumers [4, 5]. A sustained effort is required

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to enhance the power quality (PQ) of PDN, otherwise, it will affect and create different complications like damage of phase cables due to over current flow, copper loss and torque problems in the electric drive system, blackout of sophisticated equipment and overall, it degrades the whole system efficiency. All these important issues are motivating a unique research direction for the development of improved versions of DSTATCOM. Researchers and power engineers focus on reactive power compensation and harmonics control to provide quality electricity to different clients and maintain the safe and reliable operation of PDN [1-7].

Conventional two-level VSIs are widely used in universal applications due to their low cost, simplicity and reliable operation. However, a momentous amount of effort from both power engineers and researchers has gone into the design and construction of modified topology to concentrate on the issues with the conventional VSI, such as high DC link voltage, buck converter, voltage stress on switches, increase inverter rating and increase the filter inductor rating and relatively low efficiency [8-13]. To overcome the negative aspects of VSI, the topology of the T type inverter is utilized for low and medium voltage 3-phase 3-wire PDN application [14, 15]. It possesses superior reliability and better efficiency under a medium operating switching frequency range (4-30 kHz) [16-18]. Hence, T type inverters are widely applied for industrial applications such as DC power source usage, HVDC power transmission, uninterruptible power supplies, refrigeration compressors, solar systems, power grids, induction heating, electric motor speed control, etc. Not only does it enhance the PQ issues of the 3-phase 3-wire PDN under a 3-phase nonlinear load, it also increases the inverter efficiency [19-25]. But, in a recent paper, we noticed that the THD reduction in T-type inverter-based DSTATCOM is approximately equal to that of the conventional VSI based DSTATCOM [26]. The T type inverter has a unique topology configuration that supports the fault tolerance capability and other merits [16], but it is not so effective in THD reduction which is not preferred for 3-phase 3-wire PDN where quality power delivered to their clients is most important at any cost.

The PDN impedance and its characteristics regulate the performance of DSTATCOM in some applications, such as grid connected inverters and voltage control mode operation introducing an external inductor inline [27-29]. In [30], the simulation result shows the IC-T type inverter performance is better than the T type. The icos□ controller is employed for the operation of inverters [31, 32]. The control technique is authenticated by simulation results for a low and medium-voltage PDN with nonlinear load. The reference source currents are obtained from the three-phase nonlinear load current and it is found to be simple and error-free [31-34]. Additionally, the icos□ control scheme makes the proposed inverter performance better.

Of course, the complexity of the T type inverters is much more than the 2-level inverter. A 2-level inverter is not perfect for line-commutated converters (LCC). The LCC depends on the line voltage of the AC system rather than the current. In the other way, the current ripples and flow of controllability are improved by inserting an inductor in VSI. Hence, additional advantages cause the semiconductor switching devices to turn ON and OFF as per the system requirement to enhance the PQ of PDN. Finally, the findings are highlighted as fol-

lows: 1) the DC voltage regulation loop is designed to maintain DC link voltage across the capacitor, 2) the AC voltage regulation loop is designed to control AC voltage at the point of common coupling (PCC), 3) the control scheme is used to maintain source current harmonic reduction as per grid code, and 4) PF improvement is maintained.

In this paper, a 3-phase split capacitor support IC T type inverter is designed using MATLAB/Simulink software to fully exploit the benefits of the inductor coupled and T type topology. This paper identified the better DSTATCOM used for active power filtering in PDN based on the theoretical research and simulation results of conventional VSI, T type inverter, and IC-T type inverters. The designed model provides a new direction for research and development of active power filtering of 3-phase 3-wire PDN using IC-T type inverter based DSTATCOM.

This paper is arranged in the following manner: General phenomena, application, utilization and formation of the paper about IC-T type inverter under steady state and dynamic state are described in Section 1. The circuit configuration of the proposed topology is analyzed for various scenarios in Section 2. The implementation procedure of the icos□ control algorithm is given in Section 3. Simulation results justifying the feasibility of the method are presented in Section 4. Conclusions are drawn in Section 5.

2. Circuit Description of PDN and Different DSTATCOM

In this section, the structure of the proposed system is presented as follows: The PDN consists of a 3-phase nonlinear load, 3-phase balanced supply and IC-T type inverter based DSTATCOM. These various topologies based on DSTATCOM

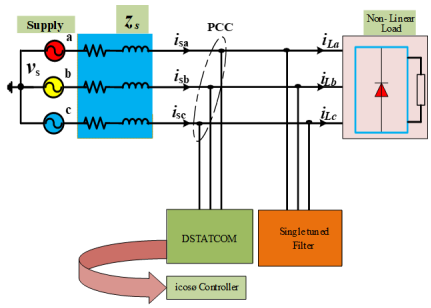

Fig. 1. Schematic diagram of 3-phase 3-wire PDN.

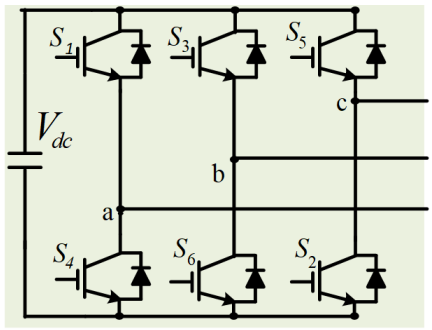

Fig. 2. Circuit configuration of two-level VSI.

are served to moderate the PQ issues, as depicted in Fig. 1. The structure of an IC-T type inverter is obtained by connecting three inductors in series with a VSI unit and a common source unit.

The different notations used in the PDN are PCC voltages of (v_{sa}, v_{sb}, v_{sc}), supply currents (i_{sa}, i_{sb}, i_{sc}), load currents (i_{la}, i_{lb}, i_{lc}), and DC link voltage (v_{dc}). In Fig. 2, the two-level VSI is shown. The T type inverter and the proposed inverter configuration are shown in Figs. 3-4, respectively. Here, an uncontrolled rectifier with resistive and inductive load is considered the same for all types of topologies. The implementation of the $i\cos\phi$ control algorithm is described as per the mathematical analysis presented in Section 3.

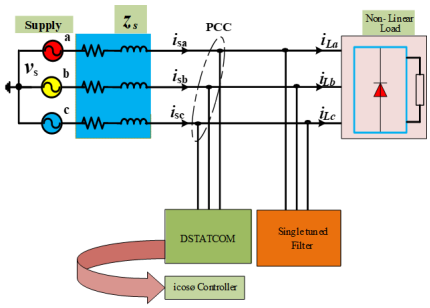

Fig. 3. Circuit configuration of T type inverter.

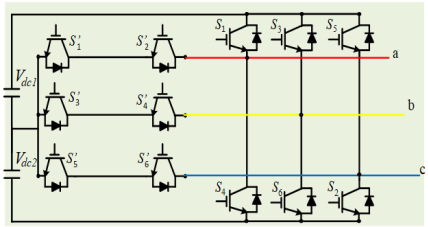

Fig. 4. Circuit configuration of IC-T type inverter.

2.1 Novelty of the IC-T type inverter

The authors are motivated to develop a new topology for achieving fault tolerant and reactive power control capability in PDN. The novelties of the IC-T type inverter with the proposed $i\cos\phi$ controlled method are as follows.

2.1.1 Increase the overload capacity of the inverter

The total load current supplied by the IC-T type inverter is equal to the summation of currents provided by the VSI and common source. Therefore, the current rating of switches is decreased. Hence, the inverter overload capability can be boosted due to unexpected continuous overload conditions [16].

2.1.2 Reduced DC link voltage

The IC-T type inverter DC link voltage is reduced by approximately 5% from 690V to 660V, as compared to VSI [26, 30].

2.1.3 Reduction in THD of the supply current

The %THD of the source current obtained from the proposed inverter is less as compared to other topologies [26, 30].

2.1.4 Merits of the modular configuration

The proposed system possesses less THD of the source currents. Also, the modular configuration of the proposed inverter provides fault-tolerant capability which increases the reliability of the inverter. The reliability of the inverter has been given more importance than harmonic distortions, especially in sophisticated equipment connected to PDN [16-18].

2.1.5 Better efficiency than VSI

The T type inverter has higher reliability and efficiency for the medium operating switching frequency (4-30 kHz) [16-18] and here the operating switching frequency is 20 kHz.

3. Control Algorithm

This section illustrates the operation of DSTATCOM using the icos□ control algorithm. In this proposed system operation, the source supplies the real part of the load current. Thus, in the $i\cos\phi$ control algorithm, 'i' represents the fundamental components of the connected load current and $i\cos\phi$ stands for the displacement power factor of the same load. The control structure of the recommended $i\cos\phi$ algorithm is shown in Fig. 5. Based on the principle of the $i\cos\phi$ algorithm, there are four steps to find the switching signals for controlling the DSTATCOM; these are derived below [29, 30].

- The required fundamental quantities are extracted from the load current with the help of the Fourier block.

- The unit vector templates (u_{ap}, u_{bp} & u_{cp}) are expressed using source currents (i_{sa}, i_{sb}, and i_{sc}).
- Both the active and reactive parts of load currents are processed as per the algorithm principle.
- Finally, the generated switching signals are utilised to operate the DSTATCOM for better shunt compensation.
- Design and control of the icos□ technique is briefly presented below [1].

The fundamental active components of 3- phase load currents ($i_{lap}, i_{lbp}, i_{lcp}$) are written as

$$\begin{bmatrix} i_{lap} \\ i_{lbp} \\ i_{lcp} \end{bmatrix} = \begin{bmatrix} Re(i_{la}) \\ Re(i_{lb}) \\ Re(i_{lc}) \end{bmatrix} = \begin{bmatrix} i_{la}\cos\phi_{la} \\ i_{lb}\cos\phi_{lb} \\ i_{lc}\cos\phi_{lc} \end{bmatrix}. \quad (3.1)$$

Then, the weighted active average value is

$$w_p = \left(\frac{i_{la}\cos\phi_{la} + i_{lb}\cos\phi_{lb} + i_{lc}\cos\phi_{lc}}{3} \right). \quad (3.2)$$

Further, the reactive components of fundamental three phase load currents (i_{laq}, i_{lbq}, and i_{lcq}) are obtained as

$$\begin{bmatrix} i_{lap} \\ i_{lbp} \\ i_{lcp} \end{bmatrix} = \begin{bmatrix} Im(i_{la}) \\ Im(i_{lb}) \\ Im(i_{lc}) \end{bmatrix} = \begin{bmatrix} i_{la}\sin\phi_{la} \\ i_{lb}\sin\phi_{lb} \\ i_{lc}\sin\phi_{lc} \end{bmatrix}. \quad (3.3)$$

Then, the weighted reactive average value is

$$w_p = \left(\frac{i_{la}\sin\phi_{la} + i_{lb}\sin\phi_{lb} + i_{lc}\sin\phi_{lc}}{3} \right). \quad (3.4)$$

In the design of the PI controller, there are some significant parameters to be considered such as, "w_{dp}" active components of the reference source currents,"k_{pdp}" proportional controller,"k_{idp}" integral controller, and "v_{de}" error in dc voltage.

The active components of the reference source current "w_{dp}" are the obtained from DC control loop as

$$w_{dp} = k_{pdp}v_{de} + k_{idp}\int v_{de}dt. \quad (3.5)$$

Then, the total active component of the reference supply current can be computed as

$$w_{spt} = w_{dp} + w_{lp}. \quad (3.6)$$

Further, the total reactive component of the reference supply current is expressed as

$$w_{sqt} = w_{qq} + w_{lq}. \quad (3.7)$$

The filtering weighting value of the load current is extracted with the help of a low pass filter.

Moreover, the instantaneous active and reactive source currents are expressed in Eqs. (3.8)-(3.9) respectively.

$$\begin{bmatrix} i_{sap} \\ i_{sbp} \\ i_{scp} \end{bmatrix} = w_{spt}\begin{bmatrix} u_{ap} \\ u_{bp} \\ u_{cp} \end{bmatrix}, \quad (3.8)$$

$$\begin{bmatrix} i_{saq} \\ i_{sbq} \\ i_{scq} \end{bmatrix} = w_{sqt}\begin{bmatrix} u_{aq} \\ u_{bq} \\ u_{cq} \end{bmatrix}, \quad (3.9)$$

In addition, the reference source currents are as follows:

$$\begin{bmatrix} i^*_{sa} \\ i^*_{sb} \\ i^*_{sc} \end{bmatrix} = \begin{bmatrix} i_{sap} \\ i_{sbp} \\ i_{scp} \end{bmatrix} + \begin{bmatrix} i_{saq} \\ i_{sbq} \\ i_{scq} \end{bmatrix}, \quad (3.10)$$

Both the reference ($i^*_{sa}, i^*_{sb}, i^*_{sc}$) and actual source currents (i_{sa}, i_{sb}, i_{sc}) of respective phase are compared. Then, the error signals are obtained which are processed through the hysteresis current controller (HCC). The switching devices of a-phase are controlled as:

(i) If $i_{sa} < i^*_{sa}$, the S_1 is ON and S_4 is OFF,
(ii) If $i^*_{sa} > i_{sa}$, the S_1 is OFF and S_4 is ON.

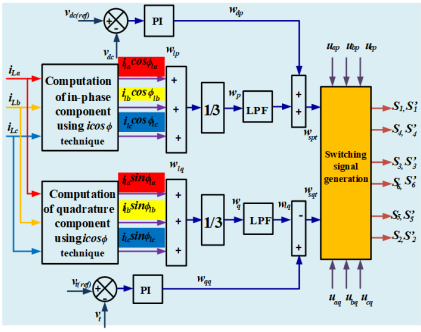

Fig. 5. Structural diagram of icos□ control algorithm.

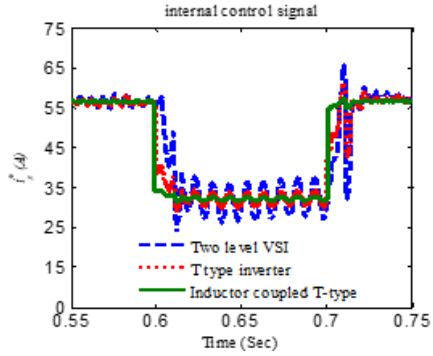

Fig. 6. Internal control signal $icos\phi$ controller.

4. Simulation Results

Fig. 1 is designed by using MATLAB/Simulink software for the above-mentioned topologies. The individual topology shunt compensation performance of source currents and power factor correction are presented in the subsequent section respectively. The different simulation parameter values of the system are arranged in Table 1. The $icos\phi$ control algorithm is used for different DSTATCOM topology operations to improve the PQ of PDN. Initially, the system is verified without DSTATCOM and it is found that the load current and source current THD are approximately equal. Next, the VSI, T type inverter and IC-T type inverter based DSTATCOM are switched ON at PCC to check its compensation capability. Internal control signals of the $icos\phi$ controller for different topologies are shown in Fig. 6. From this, it is observed that the proposed topology possesses tuned and distortionless current for producing the reference source current, which further improves the actual firing pulses required for the controlled switches.

The complete analysis of individual topology is fully discussed in the respective sub section below.

Table 1. Simulation Topology parameters.

Topology parameters	Symbol	Magnitude
DC link voltage	v_{dc}(ref)	700V
Capacitor	C_{dc}	2000μF
Proportional controller (DC)	K_{pa}	0.01
DC Integral controller	K_{ia}	0.05
Proportional controller (AC)	K_{pr}	0.2
AC Integral controller	K_{ir}	1.1
3- phase source voltage	v_s	230V (rms)/phase
Frequency	f_s	50Hz
Compensator resistance	R_c	0.25Ω
Compensator inductance	L_c	1.5mH
Source resistance	R_s	0.5Ω
Source inductance	L_s	2mH

4.1 Case-1 (VSI)

In this subsection, the case study of VSI under steady and dynamic states is executed. The simulation response from downward to upward, inverter DC link voltage, DSTATCOM compensating currents, nonlinear load currents, system source currents and system source voltage are depicted in Fig. 7. The steady state waveforms are analyzed during the time intervals T= 0.55 Sec to T= 0.6 Sec and T= 0.7 Sec to T= 0.75 Sec. The dynamic state waveforms are analyzed during the time interval, T= 0.6 Sec

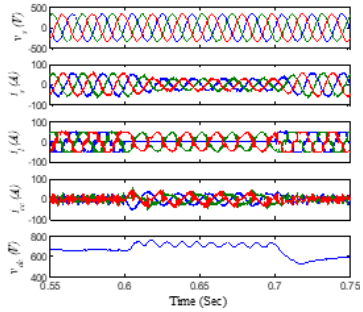

Fig. 7. Simulated waveforms under steady state and dynamic state from downward to upward, inverter DC link voltage, DSTATCOM compensating currents, non-linear load currents, system currents and system voltage.

to T= 0.7 Sec. When VSI is switched on, the stable DC link voltage of 690V is obtained during the steady state and the oscillating DC link voltage of 750V to 780V is obtained during the dynamic state. The system phase displacement between the supply voltage and current without correction before compensation and with correction after compensation are shown in Fig. 8(a)-(b) respectively. It is also noticed after compensation that the THD of the system supply currents and nonlinear load currents are 4.69% and 34.82% shown in Fig. 8(c)-(d).

4.2 Case-2 (T type inverter)

In this subsection, the case study of the T type inverter under steady and dynamic states is executed. The simulation response from downward to upward, inverter DC link voltage, DSTATCOM compensating currents, non-linear load currents, system source currents and system source voltage are depicted in Fig. 9. The steady state waveforms are analyzed during the time intervals T= 0.55 Sec to T= 0.6 Sec and T= 0.7 Sec to T= 0.75 Sec. The dynamic state waveforms are analyzed during the time interval, T= 0.6 Sec to T= 0.7 Sec. When the T type inverter is switched on, the sta-

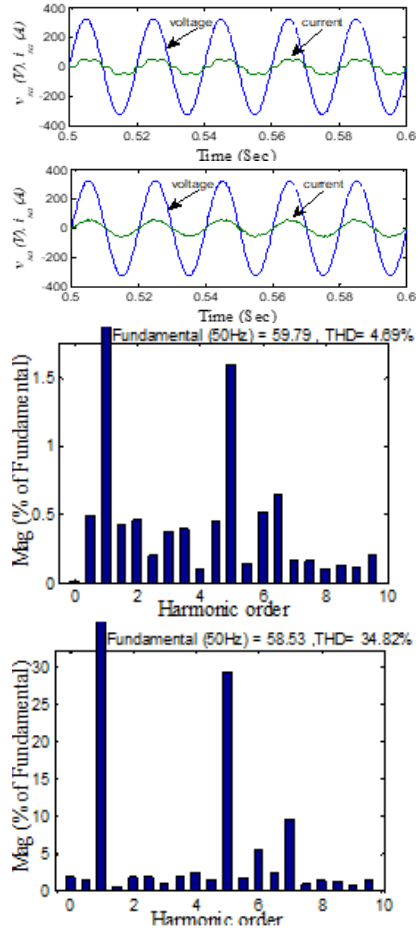

Fig. 8. Simulated system power factor without correction.

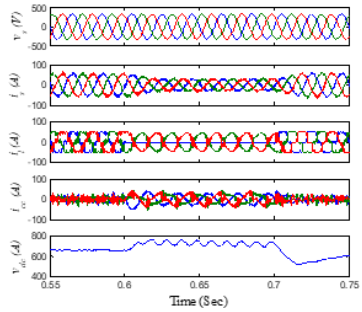

Fig. 9. Simulated waveforms under steady state and dynamic state from downward to upward, inverter DC link voltage, DSTATCOM compensating currents, non-linear load currents, system currents and system voltage.

ble DC link voltage 680V is obtained during the steady state and the oscillating DC link voltage 735V to 760V is obtained during the dynamic state. The system phase displacement between supply voltage and current without correction before compensation and with correction after compensation are shown in Fig. 10(a)-(b). It is also noticed after compensation that the THD of the system supply currents and nonlinear load currents are 4.80% and 35.23% shown in Fig. 10(c)-(d).

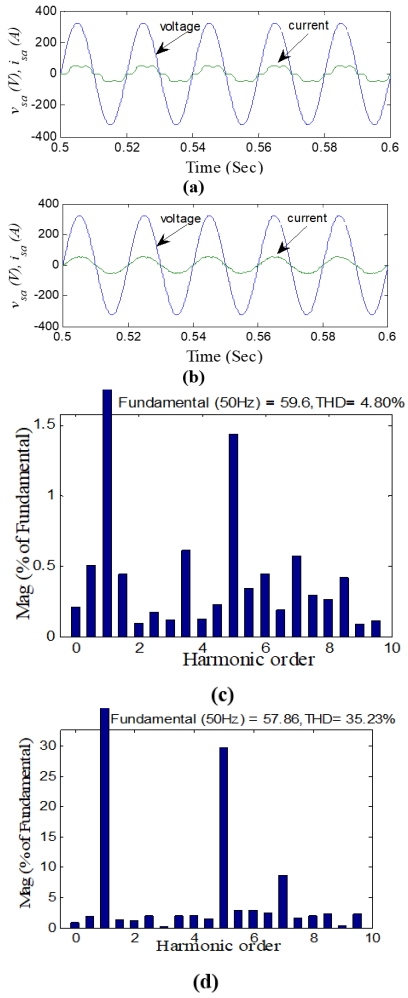

Fig. 10. Simulated system THD% of load current.

4.3 Case-3 (IC-T type inverter)

In this subsection, the case study of the IC-T type inverter under steady and dynamic states is executed. The simulation response from downward to upward, inverter DC link voltage, DSTATCOM compensating currents, non-linear load currents, system source currents and system source voltage are depicted in Fig. 11.

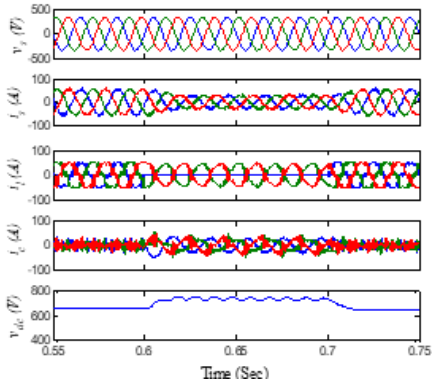

Fig. 11. Simulated waveforms under steady state and dynamic state from downward to upward, inverter DC link voltage, DSTATCOM compensating currents, non-linear load currents, system currents and system voltage.

The steady state waveforms are analyzed during the time intervals T= 0.55 Sec to T= 0.6 Sec and T= 0.7 Sec to T= 0.75 Sec. The dynamic state waveforms are analyzed during the time interval, T= 0.6 Sec to T= 0.7 Sec. When IC-T type inverter is switched on, the stable DC link voltage 660V is obtained during steady state and the oscillating DC link voltage 715V to 740V is obtained during the dynamic state. The system phase displacement between the supply voltage and current without correction before compensation and with correction after compensation are shown in Fig. 12(a)-(b). It is also noticed after compensation that the THD of the system supply currents and nonlinear load currents are 3.15% and 34.37% shown in Fig. 12(c)-(d). The IC-T type

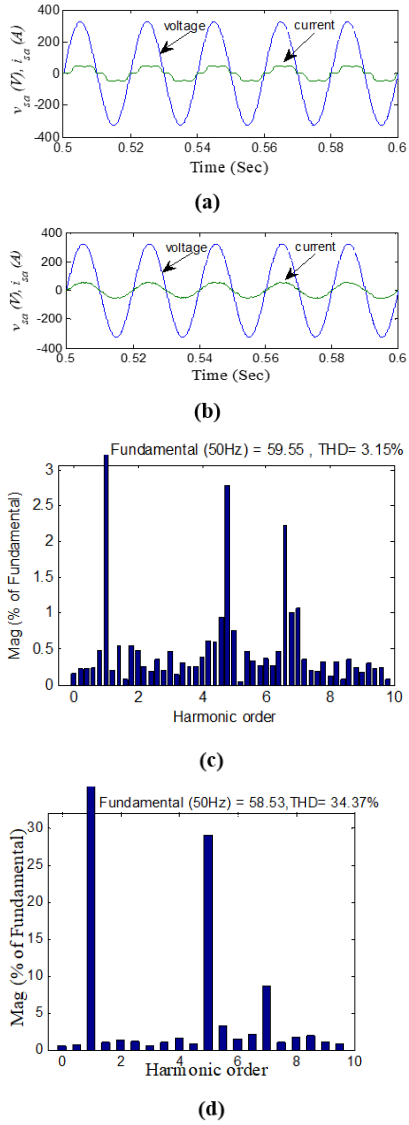

Fig. 12. Simulated system THD% of load current.

inverter is compared with VSI and T type inverter and their performed simulation results are arranged in Table 2. The obtained results compared with the existing ones are presented Table 3.

5. Summary

In this paper, the shunt compensation capability of IC-T type inverter for enhancing PQ in PDN is presented in detail. Compared to the VSI and T type topology, the IC-T type inverter inherits the advantages which are detailed below.

- Source current THD reduction is performing satisfactorily during compensation within the limit of grid connection standard
- The proposed system is found to be capable of delivering the power with improved P.F. according to the availability on the source side.
- The issue of poor voltage regulation is mitigated, thus ensuring stable operation of the PDN.
- The switching power loss is reduced, which demonstrates its superiority over the aforementioned topologies.
- Maintains the DC link voltage at the desired level (less than from VSI and T type inverter).

The obtained simulation results are in

Table 2. Performance parameters of VSI, T type inverter and IC-Ttype inverter.

Performance parameter	DSTATCOM at PCC		
	VSI	T type inverter	IC-T type inverter
Source Current(A), %THD	59.79, 4.69	59.6, 4.80	59.55, 3.15
Source Voltage (V), %THD	321.4, 2.23	321, 1.42	321.4, 1.04
Load current (A), %THD	58.53, 34.82	57.86,35.23	58.53, 34.37
P. F	0.96	0.94	0.98
DC link voltage (V)	690	680	660
Fault tolerant capability	No	Yes	Yes
Over load capability of inverter	No	Up to 20% of rated load	Up to 20% of rated load
Protection of sophisticated equipment	NO	Yes (modular configuration)	Yes (modular configuration)

Table 3. Comparison of proposed work result with existing one.

Measurement	Source current THD%	P.F
Reference [1]	4.14	0.9
Proposed work results	3.15	0.98

close agreement with those theoretically derived. The inference made from these above shows that the recommended DSTATCOM is the suitable shunt compensator for PDN.

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