# Design of a High Gain Low Noise Amplifier at 3.3 GHz using CMOS Technology

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Received April 29, 2024, Revised May 30, 2024, Accepted June 24, 2024, Published December 17, 2024

**Abstract.** *Low noise amplifier (LNA) is the important device used in field of communication. The main objective of this device is to boost the level of low power signal to a sufficient level without altering the signal to noise ratio in the circuit. This paper proposes a novel LNA with improved gain and optimized noise figure using Gain Enhancement and Image Rejection (GEIR) technique. CMOS technology is used in proposed work. LNA using CMOS at 90 nm technology is proposed using image rejection. The proposed amplifier boosts signal amplification using a 4 transistor CMOS GEIR network by providing proper input and output impedance matching. Simulations are performed using Cadence tool. The proposed amplifier is operating at a center frequency of 3.3 GHz and is able to achieve 14.5 dB gain and low noise figure. This could be useful in WIMAX application where high speed data rate at wide area coverage is required.*

## Keywords:

Low noise amplifier, CMOS, 5G communication, inductor, image rejection

## 1. Introduction

A LNA is used to boosts weak signals without adding extra noise. The primary goal of an LNA is to amplify weak signals effectively. Forward body biasing [1] and current reuse [2] is the methods available to reduce power consumption in low-noise amplifiers, reducing the threshold voltage of MOS transistor. The gain of LNAs can be reduced under low DC power. It is important to consider characteristics of LNA for better output. Gain is the important parameter that measures how much larger the output signal is compared to the input signal typically expressed as ratio in decibels [3]. A higher gain is desired in an LNA to boost the weak signals which inturn improves the signal power and hence improved Signal to Noise Ratio (SNR) at the output. Noise figure measure quantifies how much the LNA contributes to the overall system noise. Low noise figure indicates better performance and introduces less noise. Bandwidth is another important parameter in design of LNA. It is the range of frequencies over which the LNA can effectively amplify signals [4]. The bandwidth of designed LNA must be chosen based on frequency of signals of interest. Narrowband and wideband LNAs are popular for the respective applications. While deigning the power consumption requirement is to be checked. It indicates the electrical power used by the LNA. Minimizing power consumption is crucial in battery operated devices. Noise temperature in important parameter related to noise performance of LNA. Low noise temperature indicates better noise performance I, especially in radio astronomy and other sensitive applications.

### *A. Design methodologies of Low Noise Amplifiers*

LNAs are designed using different topologies. The cascode LNA is a low noise amplifier having two stages, which consists of a common emitter stage and common base stage. The main advantage of cascode LNA is the good gain and better noise performance [5]. So it is suitable for very high frequency applications. This structure mainly consists of CE amplifier for voltage gain improvement and the other stage contains common base. The output of common emitter stage is connected to the base of common-base amplifier in second stage [6]. The common base configuration provides low input impedance improving the matching with preceding stage and reducing the miller effect [3]. The next topology uses feedback LNA which uses feedback techniques to enhance their performance. The advantage of feedback is that it controls the gain and bandwidth while maintaining low noise levels [7]. These are useful for precise control over the parameters. A differential LNA configuration is used. This configuration contains pair of transistors and is benefitted for common mode noise rejection and improved linearity [8]. It is mostly used in situations where noise rejection is critical. Based on operating temperature specific cryogenic LNAs are available in literature [9-14].

## 2. State of Art Methods

This work utilizes variable frequency, image-rejection technology for providing low power and low noise. LNA [1] used 0.4 V supply voltage for designing TSMC CMOS technology. In [4] LNA at 2 GHz is discussed which provides a power gain of 15 dB and noise figure of 5.5 dB and an 3$^{rd}$ order intercept point of 13 dBm [4]. For

simultaneous power gain improvement and variable frequency image rejection [10], the LNA with variable capacitor and inductor is proposed. The image rejection frequency varies between 3 and 3.6 GHz and measured IRR spans from 14-39 dB [4]. In [5] it is proposed a low power LNA at 6 GHz frequency incorporates active and passive transconductance improvement [11]. It achieves a balance of high gain, low noise figures and minimal power consumption [12]. It is proposed in Global Foundries 0.18 micrometer technology node. It demonstrates a gain of 14.5 dB at a frequency of 5.8 GHz [6].

Later folded cascade topology is incorporated using both active elements as well as passive elements for transconductance improvement [13]. It operates at 0.5 voltage and consumes a power of 0.87 mW. In [14] discusses the design and performance of CMOS based LNA which uses a self-bias and body floating techniques for $5^{th}$ generation systems [15] uses 6 GHz frequency. In [15] the LNA is capable of providing a voltage gain of 9.4 dB approximately at a Vdd of 0.8 V uses a power of 1.36 mW. The self-bias body floating technique involves connection between body of transistor and drain through resistance parameter, resulting on improved performance and reduced leakage current. In [15] the cascode stage is followed by common source as buffer stage and incorporates inductors and transmission lines to reduce resistive loss. The LNA demonstrates good input matching (S11) and achieves a bandwidth of 9.6 GHz.

Development of LNA for GPS applications is discussed [8]. The LNA has a NF of 0.5 dB and an IIP3 of 2.91 dBm. The frequency of operation is 1.57 GHz and has a power consumption of 8.7 mW for a 1.5 V supply. This LNA uses cascode topology with cascade transistor for isolation and operates in the sub-threshold region. The LNA has been designed using UMC 90nm library and shows better power gain and noise figure.

Noise matching network improves the noise characteristics and improve noise figure for mid-band 5G applications. Performance of LNAs using high pass and low pass filter structures are studied [6]. High pass Filter structure uses higher DC power usage and achieves better noise figures when compared to Low pass filter structure. A peak gain 0f 14.19 dB and input compression is achieved [6]. The intercept point of -12 dBm and +2.0 dBm. In [13] LNA provides low, flat noise figure around 3.2 dB and high flat power gain around 12 dB over the frequency range is achieved. The LNA [13] consumes 9.96 mW and has a chip area of 0.813x0.883 mm2, making it suitable for wideband communication systems. The LNA with parallel LC load and shunt feedback configuration achieves wide band impedance matching at input side. The LNA has a 7.44 GHz/mW FOM, which is best value for an LNA and good bandwidth. LNA in [14] developed for wireless communication utilizes a Noise Cancellation technique to reduce noise and improve performance. It is a two stage design proposed, in which the CS amplifier amplifies the signal while the CG amplifier cancels out the noise. It is designed using CMOS technology operates at 1 GHz to 1.8 GHz frequency range.

In [16] low noise amplifier at Ku band using 65 nano meter bulk CMOS technology is developed. It uses a two stage cascade configuration and achieves improved gain. The LNA uses 22mW power with a 1 volt supply voltage and gate bias voltages. It has a gain of over 17.7 dB and a NF of 1.66 to 2.13 dB around 16 GHz range. It uses a gate inductor in series connection for input along with proper noise matching. In [11] 180 nm CMOS X-band LNA at both room temperature and cryogenic temperature is proposed. The LNA developed effectively matches input and output impedances within the band of 6-7 GHz at both temperatures. The LNA contains gain of approximately 18 dB and works at 78 K temperature. [13] uses a shunt inductor for ESD protection, but results in deterioration of the noise figure performance. It shows the potential for space applications. In [12] a cryo LNA is proposed for astronomy receivers. It is fabricated with 65-nm bulk CMOS technology and operates at 20 K with power consumption of 115 mW.

## 3. Proposed Low Noise Amplifier

This LNA uses the latest CMOS technology to reduce power consumption and power dissipation of NMOS and PMOS transistors. The linearity of proposed design is improved by providing the accurate input impedance matching and output impedance matching networks. The performance of low noise amplifier is that a gain of 10-30 dB and a noise figure of 3-5 dB. The matching networks are shown in Fig.1. The impedance matching network at input contains a capacitor, MOS transistors and two inductors. PMOS, Capacitor and two inductors are used at output network. The main core consists of Gain Enhancement Image Rejection (GEIR) circuit with 4 transistors connected in cascade. Each cascade connection consists of MOS transistor and a capacitor.

The proposed LNA consists of three important sections. They are impedance matching network sections at input and output, GEIR sections. The impedance matching network at input consists of one NMOS transistor, blocking capacitor $C_g$ and $C_s$ and Ls are used for reducing reflections. $R_g$ resistor is used for providing proper biasing. The input impedance is matched with 50 ohms. A PMOS transistor is used at output impedance matching network. $C_0$ is used to block DC current. $L_b$ and $L_0$ are used for reducing any reflections present at output. The output impedance is matched with 50 ohms. GEIR consists of 4 NMOS cascaded transistors and a voltage of 0.4 v is applied at gate terminals of transistors. This provides gain enhancement without disturbing linearity.

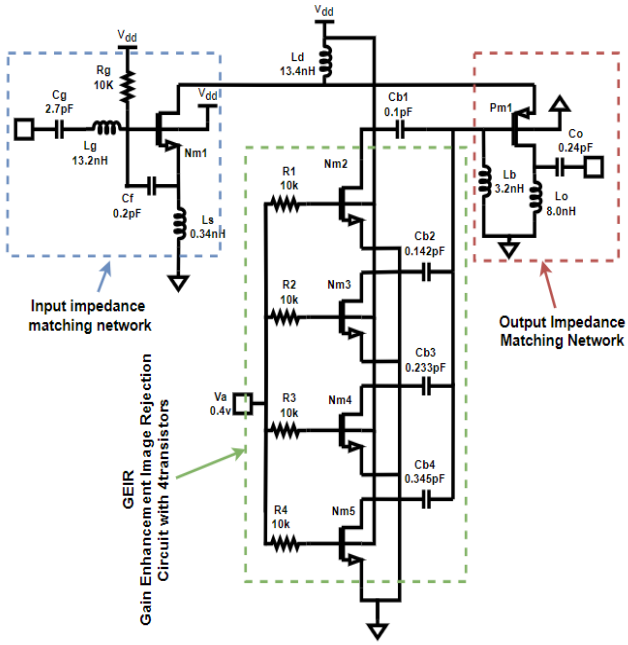


**Fig. 1** Implemented Circuit Diagram

GEIR refers to the technique used to increase the amplification in LNA without significantly degrading its performance in terms of noise figure, linearity, and power consumption. Multi-Stage Amplification is used in this technique. Cascading multiple amplifier stages can significantly increase the overall gain. Each stage provides a moderate gain, but when combined, they offer high total gain. Image frequency can produce unwanted signals that fall within the pass band of the IF filter, causing interference. Image rejection techniques prevent interference from unwanted signals, ensuring that the desired signal is accurately extracted and processed. Therefore, effective image rejection is necessary to eliminate these unwanted signals. Gain enhancement techniques ensure that the LNA provides sufficient signal amplification while maintaining low noise and high linearity. Both gain enhancement and image rejection are essential for optimizing the performance of LNAs in communication systems. Here the feedback connection is responsible for image rejection.

## 4. Simulation Results

The proposed LNA is simulated in CADENCE virtuoso tool. The libraries are available at gpdk90. The performance is analyzed using performance measures S11, Gain and noise figure. Comparison of proposed method with existing methods is shown in Tabel 1. The results for $S_{11}$, measures the return loss at input is given in Fig.2, Figure 3,4 and 5 provides the s parameters. Figure 6 shows the noise figure performance curve.

The proposed work is compared using performance measures supply voltage, gain, $S_{11}$ and noise figure. It is seen that the LNA provides better gain and image rejection compared to existed methods. As the proposed method utilizes less voltage supply of 0.4 V, low power is utilized by the circuit. A gain of 14.3 dB is achieved at an operating frequency of 3.3 GHz. $S_{11}$ shows the image rejection capability of proposed method while maintaining good gain and linearity than other existing methods.

**Table 1** Comparison of proposed work

| Parameter | This Work | [4] | [5] | [6] | [7] |
|---|---|---|---|---|---|
| CMOS(nm) | 90 | 180 | 180 | 180 | 180 |
| Frequency (GHz) | 3.3 | 5.0 | 5.8 | 2.8 to 4.5 | 2.4 |
| Supply Voltage (V) | 0.4 | 0.63 | 0.5 | 0.9 | 0.4 |
| S11 (dB) | -22.1 | -14.5 | -14.7 | -13.9 | -13.9 |
| Gain (dB) | 14.3 | 21.4 | 14.2 | 14.19 | 15 |
| Noise Figure (dB) | 4.52 | 4.1 | 3.2 | 2.6 | 2.6 |

The simulations are performed at a temperature of 27°C. Industry standard for designing low noise amplifier uses minimum $S_{11}$ of 10 dB, Gain between 10 to 15 dB and NF between 0.5 to 5 dB. Our proposed method provides the values on par with industry standards. A power supply of 0.4 v is used for circuit operation. Transistor parameters are used as follows Table 2.

**Table 2** Transistor parameters

| Transistor | Width (µm) | Length (nm) |
|---|---|---|
| Nm1 | 30 | 100 |
| Nm2 | 30 | 180 |
| Nm3 | 30 | 100 |
| Nm4 | 30 | 100 |
| Pm1 | 30 | 100 |

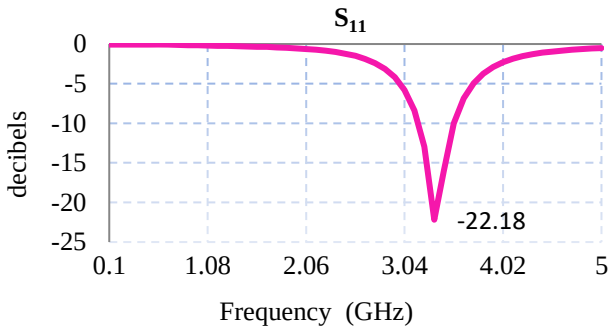


**Fig.2** $S_{11}$ of the designed LNA.

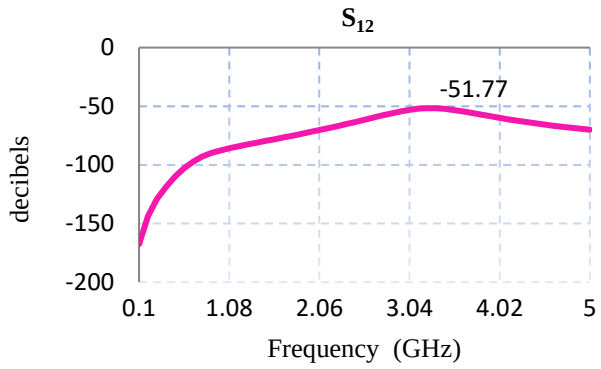


**Fig. 3** $S_{12}$ of the designed LNA.

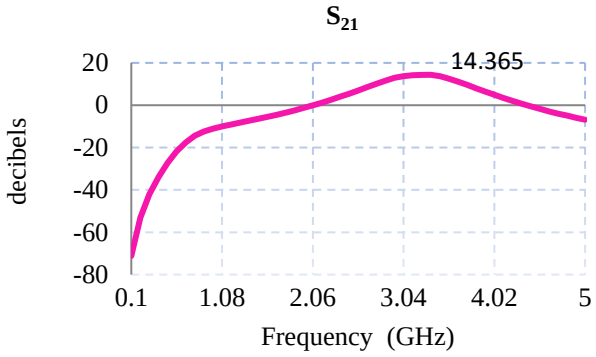


**Fig.4** $S_{21}$ of the designed LNA.

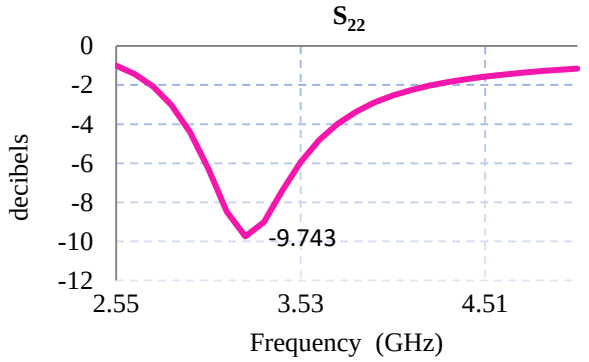


**Fig.5** $S_{22}$ of the designed LNA.

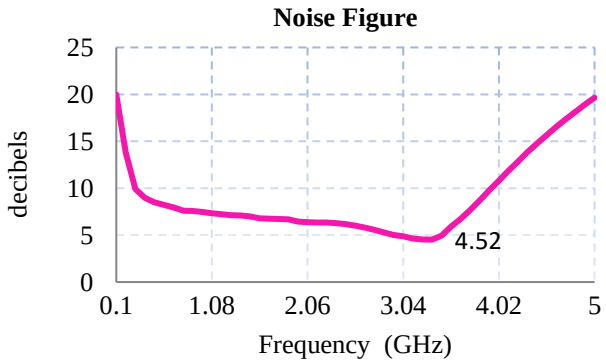


**Fig. 6** Noise Figure of the designed LNA.

In this work Gain Enhancement and Image Rejection (GEIR) based LNA is proposed. This provides image rejection and gain enhancement without deviation in linearity. The linearity is observed from $S_{11}$ graph. Proposed method provides a gain of 14.3 dB and a noise figure of 4.52 dB. The frequency of operation of proposed LNA is around 3.3 GHz.

## 5. Conclusion

In this study we successfully examined the low noise amplifier using GEIR approach at 0.4V. Low Noise amplifier in 90nm CMOS technology is developed in this work. GEIR based gain improvement circuit has been proposed and analyzed the performance. The LNA is operating at 3.3GHz. The application at this frequency is used in WIMAX, which is used to provide high speed data rate at a wide area. The proposed LNA is suitable for low noise and low power applications.

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